APPLYING HIGH-PERFORMANCE MONOLITHIC FET-INPUT OP AMPS

Super Singles and Duals Use New Trimmed Bipolar-FET Technology

The Ideal Op Amp Still Doesn't Exist, But These Come Close Enough

by Don Travers

From the earliest days of the monolithic operational amplifier, new amplifier chips have come to market with continually improving performance. As refinements to existing technologies and manufacturing processing techniques evolve, total operational-amplifier performance approaches that of an ideal amplifier ever more closely, for most practical purposes. Refinements to bipolar operational amplifier processing involving ion-implanted FETs (in some cases called "Bi-FET" techniques), in particular, have narrowed the gap between practical and ideal amplifiers in dc performance without sacrificing bandwidth.

For example, it is now possible to trim single and dual FET-input monolithic op amps for both minimum drift and minimum offset—automatically, at the wafer stage. The improvement in overall performance is a boon to users, simplifying many designs and providing high accuracy at reduced cost.

Here are a few examples of the kind of performance available in off-the-shelf devices: the drift-trimmed AD547LH has maximum offset and drift of 0.25mV and 1μV/°C, open-loop gain of 250,000V/V, and bias current of 25pA max, *at operating temperature*; and the wider-bandwidth AD544LH has 2MHz bandwidth and 13V/μs slewing rate, with maximum offset and drift of 0.5mV and 5μV/°C. Table 1 outlines the salient properties of the op amps in this series.

Applications requiring excellent dc performance at low cost call for the AD542* and AD547* monolithic FET operational amplifier families and the equivalent duals—AD642* and AD647*. For example, precision instrument front ends, requiring accurate amplification of millivolt-level signals from megohm source impedances, will benefit from the devices' combination of low offset voltage and drift, low bias current, and low 1/f noise. The dual versions of these amplifiers, since they are closely matched, are ideal for true instrumentation amplifiers and log-ratio amplifiers.

The AD544* family of single op amps and the AD644* family of equivalent dual op amps are recommended for any application requiring excellent dynamic—in addition to dc—performance. The wide bandwidth, low offset voltage, and high open-loop gain ensure superior accuracy in high-impedance buffer and sample-and-hold applications. The AD644, with matched amplifiers, can be used for wide-bandwidth instrumentation amplifiers, low-dc-drift active filters, and as output amplifiers for four-quadrant multiplying d/a converters, such as the AD7541A 12-bit CMOS DAC.

In these pages, we will show you some concrete examples of popular op-amp applications that benefit from the improvements in precision monolithic FET-input op amp technology and will offer suggestions for obtaining best results. The applications include operations with d/a converters and sensors, practical log amps, and high-input-impedance instrumentation amplifier circuits.†

D/A CONVERTER APPLICATIONS

CMOS multiplying DACs, from the earliest 10-bit AD7520 to the modern 16-bit AD7546, rely on op amps for interfacing and buffering. For the best linearity and most stable dynamics, the choice of op amps is by no means trivial‡

CMOS DACs will provide improved overall performance when used with amplifiers in this series to perform both 2-quadrant and 4-quadrant operations. For example, the output impedance of a CMOS DAC varies with the bit composition of the digital word, affecting the noise gain ($1 + R_F/R_o$, where R_o is the resistance between OUT1 and common) of the amplifier circuit. The effect is to cause a nonlinearity, the magnitude of which is is dependent on the offset voltage of the amplifier and its drift over the operating temperature range.

TABLE 1. Monolithic Bipolar Fet Op Amps
(Typical specifications at 25°C and rated supply unless noted otherwise)

Model[1]	Gain min V/V	Bandwidth Unity Gain MHz	Slewing Rate V/μs	Settling Time(0.01%) μs	Offset max. mV	Voltage Drift, max μV/°C	I_{BIAS} max warm pA
SINGLE AMPLIFIERS							
AD542JH	100k	1.0	3.0	5.0	2.0	20	50
AD542KH	250k	1.0	3.0	5.0	1.0	10	25
AD542LH	250k	1.0	3.0	5.0	0.5	5	25
AD542SH	250k	1.0	3.0	5.0	1.0	15	25
AD544JH	30k	2.0	13	3.0	2.0	20	50
AD544KH	50k	2.0	13	3.0	1.0	10	25
AD544LH	50k	2.0	13	3.0	0.5	5	25
AD544SH	50k	2.0	13	3.0	1.0	15	25
AD547JH	100k	1.0	3.0	5.0	1.0	5	50
AD547KH	250k	1.0	3.0	5.0	0.5	2	25
AD547LH	250k	1.0	3.0	5.0	0.25	1	25
AD547SH	250k	1.0	3.0	5.0	0.5	5	25

DUAL OP AMPS					Each Side	Match	Each (Note 2)	Match	Each Side	Match
AD642JH	100k	1.0	3.0	5.0	2.0	1.0	3.5	3.5	75	35
AD642KH	250k	1.0	3.0	5.0	1.0	0.5	2.0	2.0	35	25
AD642LH	250k	1.0	3.0	5.0	0.5	0.25	1.0	1.0	35	25
AD642SH	250k	1.0	3.0	5.0	1.0	0.5	3.5	3.5	35	35
							(Note 2)			
AD644JH	30k	2.0	13	3.0	2.0	1.0	3.5	3.5	75	35
AD644KH	50k	2.0	13	3.0	1.0	0.5	2.0	2.0	35	25
AD644LH	50k	2.0	13	3.0	0.5	0.25	1.0	1.0	35	25
AD644SH	50k	2.0	13	3.0	1.0	0.5	3.5	3.5	35	35
							(μV/°C max)			
AD647JH	100k	1.0	3.0	5.0	1.0	1.0	10	10	75	35
AD647KH	250k	1.0	3.0	5.0	0.5	0.5	5	5	35	25
AD647LH	250k	1.0	3.0	5.0	0.25	0.25	2.5	2.5	35	25
AD647SH	250k	1.0	3.0	5.0	0.5	0.5	10	10	35	25

Notes:
[1] J, K, L suffixes denote 0° to 70°C operation; S denotes −55°C to +125°C; H denotes the hermetically sealed 8-pin TO-99 package.
[2] Maximum drift between T_{min} and T_{max}, mV.

For example, in the one-bit code transition from 0011 1111 1111 to 0010 0000 0000, the output offset voltage changes from $2V_{os}$ to $(4/3)V_{os}$, a change of $(2/3)V_{os}$. If V_{os} is not much smaller than the voltage equivalent of the least-significant bit, and is of the right (wrong) polarity, the transition will be nonmonotonic. This factor is especially important in multiplying applications, where the reference input can be considerably less than full scale, and the bit voltage accordingly quite small.

These monolithic FETs, with their trimmed offset and low drift,

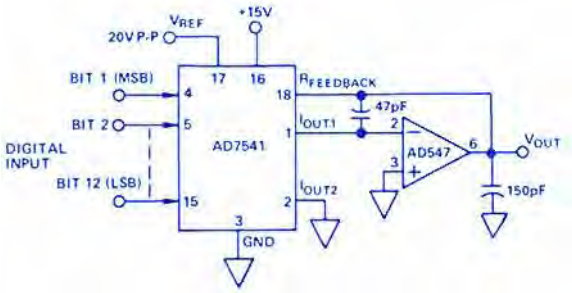
*Use the reply card for technical data.

†This article is condensed from material collected for an Application Note on monolithic FET-input op amps of the above series. For a copy of the complete A/N when available, use the reply card.

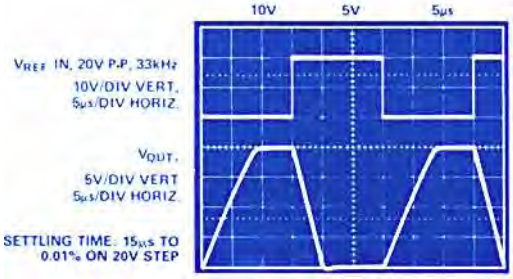
‡For information on the interaction between op amp and DAC, see "Analog Signal Handling for High Speed and Accuracy," *Analog Dialogue* 11-2, pages 11 & 12.

will minimize this effect. In addition, DAC output circuits using these monolithic FET op amps do not require the Schottky diodes that are recommended for protection of many older CMOS DAC types from amplifier turn-on transients.

Figure 1a shows the AD547 op amp and AD7541 CMOS d/a converter configured for unipolar binary (2-quadrant-multiplying) operation. With a dc reference voltage or current, of either positive or negative polarity, applied at pin 17 of the DAC, the circuit operates as a unipolar fixed-reference converter. With an ac reference voltage or current, the circuit provides two-quadrant multiplication (digitally controlled attenuation).



a. AD547 used as DAC output amplifier.

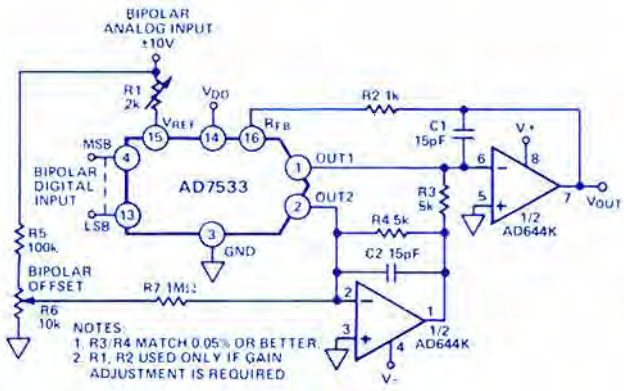


b. Response to ± 20V p-p reference square wave.

Figure 1. Voltage-output multiplying DAC.

The oscilloscope photos of Figure 1b show the output of the circuit of Figure 1a. The upper trace represents the ac reference input, a 20V peak-to-peak square wave at 33kHz, and the lower trace shows the output voltage while the digital input to the DAC is all-1's (gain of $1 - 2^{-n}$), representing a settling time to 0.01% of 15µs, with well-behaved dynamics. The 47pF capacitor across the feedback resistor compensates for the DAC output capacitance, and the 150pF load capacitor serves to reduce signal feedthrough spikes at the output.

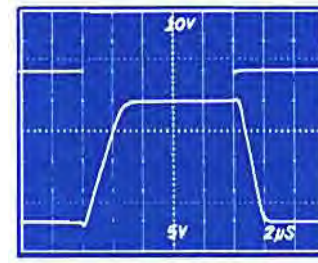
The diagram of Figure 2a illustrates the 10-bit digital-to-analog converter, AD7533, connected for bipolar operation. Since the digital input can accept bipolar numbers and V_{REF} can accept a bipolar analog input, the circuit performs 4-quadrant multiplication.



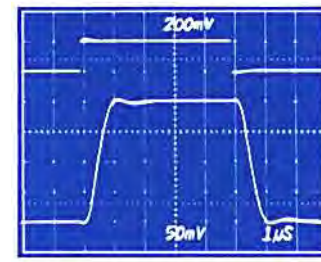
a. AD644 and AD7533 in 4-quadrant application.

This is accomplished with an AD644 dual FET-input op amp to maintain optimal performance at low cost with a low package count.

The scope plots exhibit the response to a step input at V_{REF}. Figure 2b is the large-signal response and 2c shows the small-signal response. C1, as a phase compensator (15pF), is required for stability when using high speed amplifiers; it serves to cancel the pole formed by the DAC's internal feedback resistance and the output capacitance of the DAC.



b. Large-signal response to reference square wave.



c. Small-signal response to reference square wave.

Figure 2. Four-quadrant multiplying DAC configuration.

Figure 3 shows the AD647 used with the AD7546 16-bit DAC, a two-stage device which uses 16 segmented gain levels to represent the 4 most-significant bits, a 12-bit R-2R ladder and switches for the rest, and external op amps for impedance buffering. Since 1 LSB = 8V/65536 = 122µV, in this application, amplifier performance is critical to the overall performance of the AD7546.

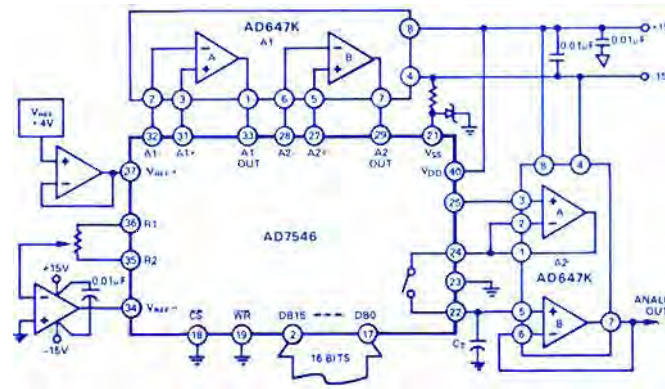


Figure 3. AD647 used with AD7546 16-bit DAC.

The paired amplifiers of A1, the AD647, are used as the high-precision dual buffer. Here, the offset voltage match, the low offset voltage and high open-loop gain of the AD647 ensure monotonicity and high linearity over the entire operating temperature range. A2, also an AD647, used as a track-and-hold, serves a dual function: amplifier A buffers the switched capacitor from the output of the ladder, and amplifier B buffers the hold capacitor from the output. The performance of the amplifiers of A2 is crucial to the accuracy of the system. Their errors are added to the errors due strictly to DAC imperfections. For this reason, great care is needed in

amplifier selection. The matching characteristics, low bias current, and low temperature coefficients of the AD647 make it ideal for this application.

Here's another DAC application where a high-performance op amp is desirable: If a CMOS DAC is connected as the feedback element in an op-amp circuit (the 8-bit µP-compatible AD7524, in Figure 4), rather than as the more-usual input element, the circuit—performing the inverse operation—will divide the input voltage by the fractional digital number, rather than multiplying by it, thus providing a repertoire of gains greater than 1. Since feedback around the amplifier is reduced, for smaller digital numbers, the gains for both signal and noise/errors are increased. Also, since the incremental step changes of gain become increasingly large for smaller values of D, in hyperbolic fashion, any errors in the gain steps, due to either DAC errors or limited open-loop gain of the op amp, are magnified correspondingly.

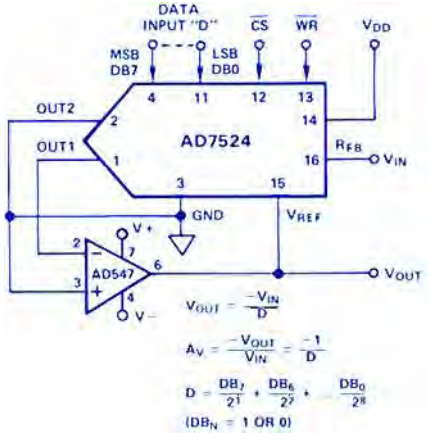


Figure 4. Analog divider with digital denominator.

As a simple analog "fix" to provide a limited gain in the extreme case of all zeros—in order to prevent the output from "taking off"—a large value of resistance (compared to $R_{FB}/2^n$) may be used to shunt the feedback path, e.g., 22MΩ. There are any number of digital fixes that may be used, in hardware or software, ranging from simply tying the LSB High to performing a logical test for all 0s—or for a number less than 1 LSB—and setting the minimum value of the digital word at 1 LSB.

INSTRUMENTATION AMPLIFIERS

When op amps are used as building blocks of high-performance instrumentation amplifiers, low drift and bias current, and high input impedance, are essential characteristics. For most instrumentation-amplifier applications, the definitive performance and low cost of the monolithic AD524 make it preferable to a user-assembled version. However, applications do exist for which the uniquely low bias current of a FET-input amplifier is essential.

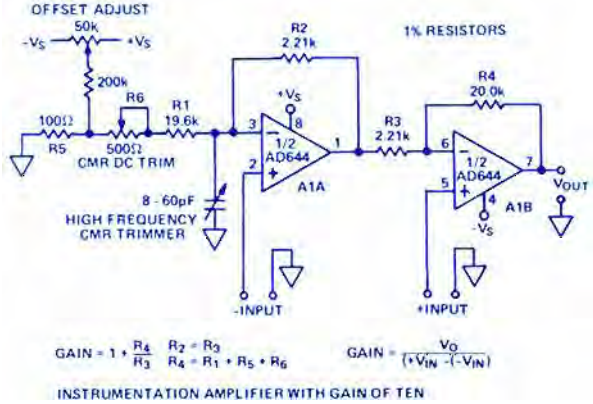


Figure 5. Wide-bandwidth instrumentation amplifier.

Figure 5 shows an easily constructed two-amplifier FET-input instrumentation amplifier employing the wider-bandwidth amplifiers in the AD644. DC offset and common-mode error are trimmable, and the CMR-trimming capacitor on the negative input of A1A permits highly accurate signal conditioning at the higher frequencies, with CMR of 80dB over the range dc to 10kHz, and bandwidth of 200kHz (−3dB) at 20V peak-to-peak output. Offset voltage drift is 10µV/°C.

The circuit of Figure 5 can be configured for a practical range of gains from less than 5 to well over 100 with typical nonlinearity of 0.01% at gain of 10. If adjustment of gain by a single resistance is desirable, a resistor, R_G, may be connected between the negative summing points, with some sacrifice in high-frequency common-mode rejection. The gain is then equal to $(1 + R_4/R_3 + 2R_4/R_G)$.

LOG-RATIO AMPLIFIERS

Log amplifiers and log-ratio amplifiers are useful in a wide variety of analog computational applications, ranging from the simple linearization of exponential transducer outputs to the use of logarithms in computations involving multi-term products or arbitrary exponents. Log amps also facilitate the compression of wide-dynamic-range analog signals into a range that can be handled without using esoteric circuit techniques.

The picoamp-level input current and low offset voltage of the AD647 make it suitable for wide-dynamic-range log amplifiers. The log-ratio circuit depicted in Figure 6, employing the AD647, can achieve less than 1% conformance error over 5 decades of current input, 1nA to 100µA. For voltage inputs, the dynamic range is typically 50mV to 10V for 1% error, limited at the low end by the amplifiers' input offset voltage, which can be reduced considerably with a pair of trim circuits like that shown in the inset.

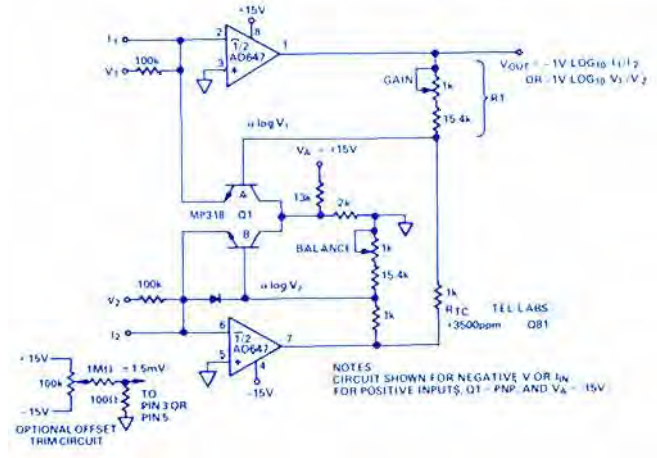


Figure 6. Log-ratio amplifier.

The conversion between current (or voltage) input and log output is accomplished by the base-emitter junctions of the high-β (greater than 100) dual transistor, Q1. If β is high, the base-emitter voltage of Q1A is, to a close approximation,

$$V_{BEA} = \frac{kT}{q} \ln \frac{I_1}{I_{SA}} \qquad (1)$$

where k is Boltzmann's constant, T is the absolute (kelvin) temperature, q is the charge on an electron, and I_{SA} is the reverse saturation current of transistor A. This circuit is arranged to take the difference of the V_{BE}'s of Q1A and Q1B, two transistors on the same

chip having matching and tracking I_S, thus producing an output voltage proportional to the log of the *ratio* of the inputs:

$$V_{OUT} = G(V_{BEA} - V_{BEB}) \quad (2)$$

$$= G\frac{kT}{q}\left(\ln\frac{I_1}{I_{SA}} - \ln\frac{I_2}{I_{SB}}\right)$$

$$= G\frac{kT}{q}\ \ln\left(\frac{I_1}{I_2}\right)$$

The scaling constant, G, is set by R1 and R_{TC} to about 16V/V, so as to produce a change of 1V in the output voltage per decade (factor-of-ten change in the ratio of the inputs). R_{TC} is a special resistor with a +3500ppm/°C temperature coefficient. Since G is inversely proportional to R_{TC}, it varies in inverse proportion to absolute temperature (T), thus compensating for changes in T. As a result, V_{OUT} is independent of temperature.

This circuit configuration is free from the dynamic problems that plague many other log circuits. The −3dB bandwidth is 50kHz for the topmost three decades, 100nA to 100μA, and decreases smoothly at lower input levels. No additional compensation is needed for stable operation with input current sources—such as photodiodes—which may have up to 100pF of shunt capacitance. For greater values of input capacitance, a 20-pF integrating capacitor around each amplifier will provide smoother frequency response.

To calibrate this log-ratio circuit, use this procedure: First apply equal voltages ($V_1 = V_2 = -10V$) and adjust "balance" for $V_{OUT} = 0.00V$. Then let $V_1 = -10V$ and $V_2 = -1V$ and adjust gain for $V_{OUT} = +1.00V$. Iterate this procedure until gain and balance errors are within 2mV of the ideal values.

SENSOR INTERFACE

In many instrumentation circuits, an operational amplifier is used as a current-to-voltage converter for the low-level output current of a sensor—which may be connected to a high-voltage source. A typical example is a flame detector in a gas chromatograph. In such applications, if there is a sensor fault condition, a very high potential may be applied to the input terminal of the operational amplifier. Some form of input protection must be used to permit the amplifier to survive the fault condition.

Some electrometer-type devices, especially, those involving CMOS circuitry, may require elaborate protection schemes employing Zener diodes. However, the protection scheme may well compromise the overall performance of the circuit, nullifying the advantages for which it was chosen in the first place. In comparison, monolithic FET amplifiers of the type discussed here do not usually require such protection, unless the source is not current-limited; in this respect, they are similar to amplifier types that use discrete JFET devices. The failure mode in such cases is overheating from excess current, rather than a voltage breakdown.

The amplifiers in this series are guaranteed for a maximum safe input potential (either common-mode or normal-mode) equal to the rated power supply voltage. The input-stage design maintains a high practical level of input resistance for differential input voltages of up to ± 1 volt. This property is useful where the amplifier is used as an open-loop comparator of two input signals, either or both of which are directly connected to high-impedance sources.

If the source is not current-limited, adequate protection can be achieved if a resistor is used, inside the loop, in series with the input terminal to limit the maximum overload current to 1.0mA (for example, 100,000 ohms for a 100-volt overload). The simple scheme shown in Figure 7 will cause no significant reduction in performance, except for bandwidth, and will provide complete dc overload protection.

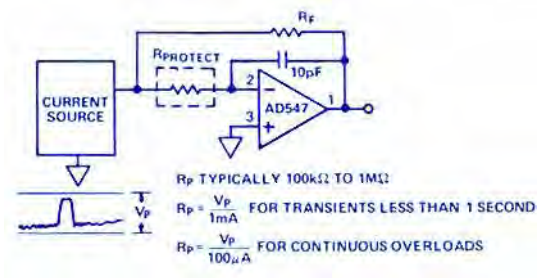


Figure 7. Input protection of I:V converter.

Output voltage of current-to-voltage converters is proportional to the value of feedback resistance (R_F in Figure 8). For greater sensitivity, increased values of feedback resistance are used (for example, 5 megohms, in Figure 9). However, beyond 10^9 ohms, resistors tend to become expensive, large, noisy, and unstable.

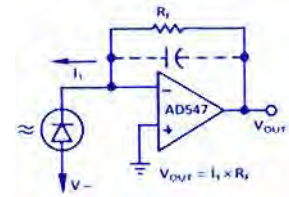


Figure 8. Photodiode amplifier – photoresistive mode.

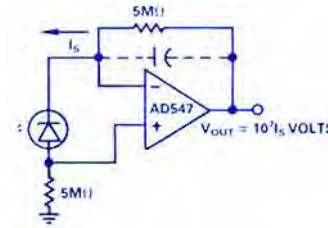


Figure 9. Photodiode amplifier – current-output photovoltaic mode.

Under some circumstances (see Figure 10), it is fruitful to use instead a high value of resistance and a low-impedance resistive divider that attenuates the portion of the output voltage used for feedback (since the signal current must now produce a smaller voltage, R_F may now be smaller than it would otherwise have had to be). For example, a 10-megohm resistor and a 1000:1 divider is nominally equivalent to a 10,000-megohm resistor. The drawback is, of course, that input voltage errors are magnified relative to the attenuated output voltage at the tap of the R1-R2 divider. The low voltage offset, drift, and noise of the AD547 enhance the attractiveness of this circuit technique.

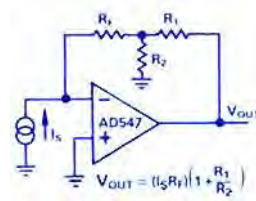


Figure 10. Current-to-voltage conversion with gain.

High-impedance transducers, such as proportional counters and some accelerometers, require an amplifier which converts an increment of charge into a change of voltage, through the use of a feed-

back capacitor. The increment of charge in circuits of the type shown in Figure 11 is obtained by variation of capacitance in a capacitive transducer sitting at constant voltage between the summing point and a voltage source. ($\Delta Q = C \cdot \Delta V + V \cdot \Delta C$, and, since $\Delta V = 0$, $\Delta Q = V \cdot \Delta C$). The op amp transfers charge to the feedback capacitor and develops the output voltage change ($\Delta V_{OUT} = -\Delta Q/C$).

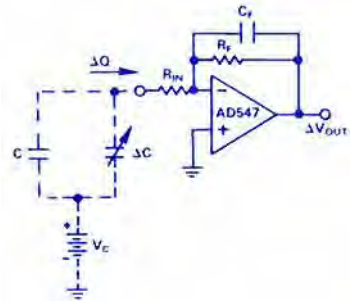


Figure 11. Charge amplifier.

In this circuit, R_F provides a leak for bias current to permit the output voltage change, due to an ac variation of charge, to be observed without excessive dc drift. The time constant, R_FC_F, should be long compared with the slowest change of charge ($1/(2\pi f_{min})$); but R_FI_{BIAS} must be small compared to the full-scale output range. R_{IN} serves to protect the amplifier's input *and output* circuit against transient and steady-state voltage breakdown in the capacitive transducer if V_C is substantial.

Applying a voltage bias to a grounded device is a common need in low-level current measurement, for example, in leakage current testing, or in using low-level current transducers (e.g., Clark oxygen sensors). Figure 12 shows a technique that applies a fixed or adjustable bias at the noninverting terminal of an op amp, thus using feedback to force the inverting terminal to the same potential. The current through the transducer is sensed by R_F, and a low-cost instrumentation amplifier converts the off-ground voltage across R_F to a single-ended output.

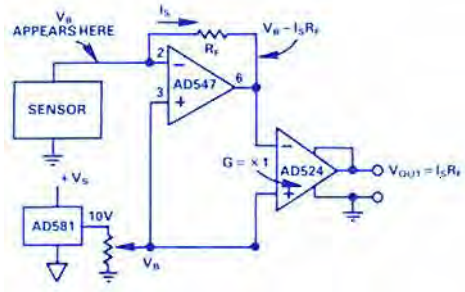
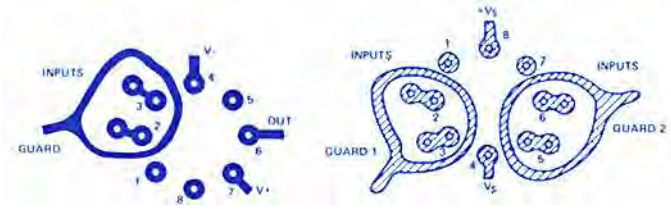


Figure 12. Current-to-voltage converter with grounded bias and sensor.

APPLICATION HINTS

The low input bias current (25pA max) and low noise characteristics of the AD547K make it suitable for electrometer applications, such as photodiode preamplifiers and picoampere-level current-to-voltage converters. In such circuits, it is essential to use guarding techniques in the design and construction of the printed circuit board layout to realize the ultimate low-leakage performance of which the amplifier is capable.

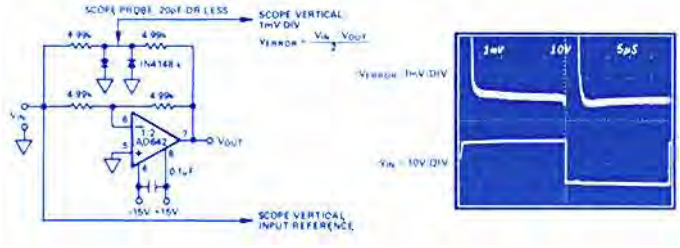
The input guarding scheme shown in Figure 13 for single and dual op amps will minimize leakage to the input circuitry from the supply terminals, the outputs, or other portions of the board wiring. The guard ring should be connected to a low-impedance potential at the same dc level as the inputs. High-impedance signal lines should be kept as short as possible; they should be surrounded by guard lines and kept away from any sources of noise and leakage. Off-board, rigid shielded cables should be used for wiring.



Single Versions Dual Versions

Figure 13. Board layout for guarding inputs.

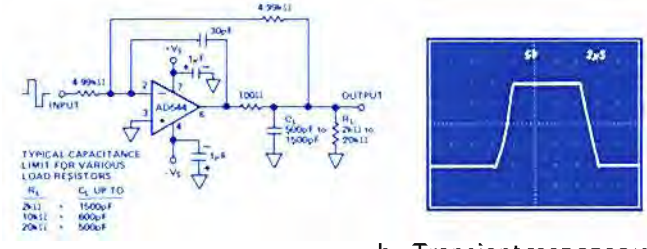
The fast settling time and low offset voltage of the the AD544 make it an excellent choice as an output amplifier for high-accuracy current-output d/a converters. The upper trace of the oscilloscope photograph in Figure 14b shows the settling characteristic of the AD544 in the circuit of Figure 14a; the lower trace is the input. Although the AD544 by itself will settle fast to within 0.01% of final output value, feedback components, circuit layout, and circuit design must be carefully considered to provide minimum settling time for the overall circuit in which it is used.



a. Test circuit b. Detail of settling characteristic.

Figure 14. Settling-time tests on AD544.

If substantial capacitive loads must be driven, they will limit the output slewing rate; In addition, the extra pole that they establish in the amplifier transfer function can be destabilizing and provide distortion, even when the circuit is being used for a low-frequency application. Improved dynamic performance can be obtained by the use of the circuit of Figure 15. A 100-ohm isolation resistor removes the capacitive load from the amplifier's output, permitting the 30pF feedback capacitor to provide phase lead in the loop. Low-frequency accuracy is maintained by closing the main loop around the 100-ohm resistor, as shown. Figure 16 shows typical transient response of this circuit.



a. Circuit b. Transient response with $R_L = 2k\Omega$ and $C_L = 500pF$.

Figure 15. Driving a large capacitive load.