

## Set 29 : Analogue multipliers

A most versatile i.c. appears in this set, incorporating four-quadrant multiplier, op-amp and buffer on the same chip, page 123, with an h.f. capability up to the order of MHz (higher in some applications). Squaring, suppressed carrier a.m., and demodulation of a.m. are uses of it shown on page 124 and page 000 (set 30) includes some further applications.

This is one of these subjects where it's difficult to avoid ending each card heading with the name of the circuit type! It is also a set containing an important class of circuit, card 8, that didn't quite do justice to its originator—Barrie Gilbert of Analog Devices. In the original card for the translinear multiplier  $R_8$  was shown wired to the wrong end of  $R_6$ . And a missing minus sign, between  $I_A$  and  $I_B$  in circuit modifications and now corrected, made nonsense of the analysis. The circuit of card 5 was originally incorrectly drawn too; inputs to  $R_{111}$  and  $R_{12}$  come from the series diode-resistor junction in the precision rectifier circuits. (Omission of  $R_2$  occurred on card 4 and, on the same card, the lower-case abbreviation  $i$  should have been shown as  $I$  to correspond with the diagrams.)

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# Introducing analogue multipliers

In the processing of electrical signals there is a need for circuits that can perform all the standard arithmetical processes – addition, subtraction, multiplication and division. The first two fall into the domain of linear amplifiers and present no great difficulty; the last-mentioned pair provide a real challenge to the ingenuity of circuit designers. Fig. 1 shows the waveforms of a particular example where an input signal  $Y$  is to be under the control of a second input  $X$ , the output being of the form  $XY$ . This is a gain-controlled amplifier and is one of the simpler forms of multiplier since usually the gain is required to be either positive or negative and not both. Hence  $X$  takes up only one polarity, and Fig. 2 shows the multiplier as needing to operate in only two of the four quadrants viz  $X$  positive,  $Y$  positive and  $X$  positive,  $Y$  negative. Such a system can be realized as in Fig. 3 where  $v_1$  corresponds to  $Y$  and  $v_2$  to  $X$ . In many such circuits it is not even essential that the gain be a linear function of  $v_2$ , in which case the circuit ceases to be a multiplier. A problem with circuits based on this idea is that of finding a resistor having negligible non-linearity over a suitable range of currents and voltages, while being controllable by an external signal.

While true and direct multiplication would be ideal, and can be obtained by using suitable transducers such as Hall-effect devices (see card 9), the designer often has to resort to devices and circuits obeying other laws. These are then manipulated until some combination of them yields a term which is proportional to the product of two signals.

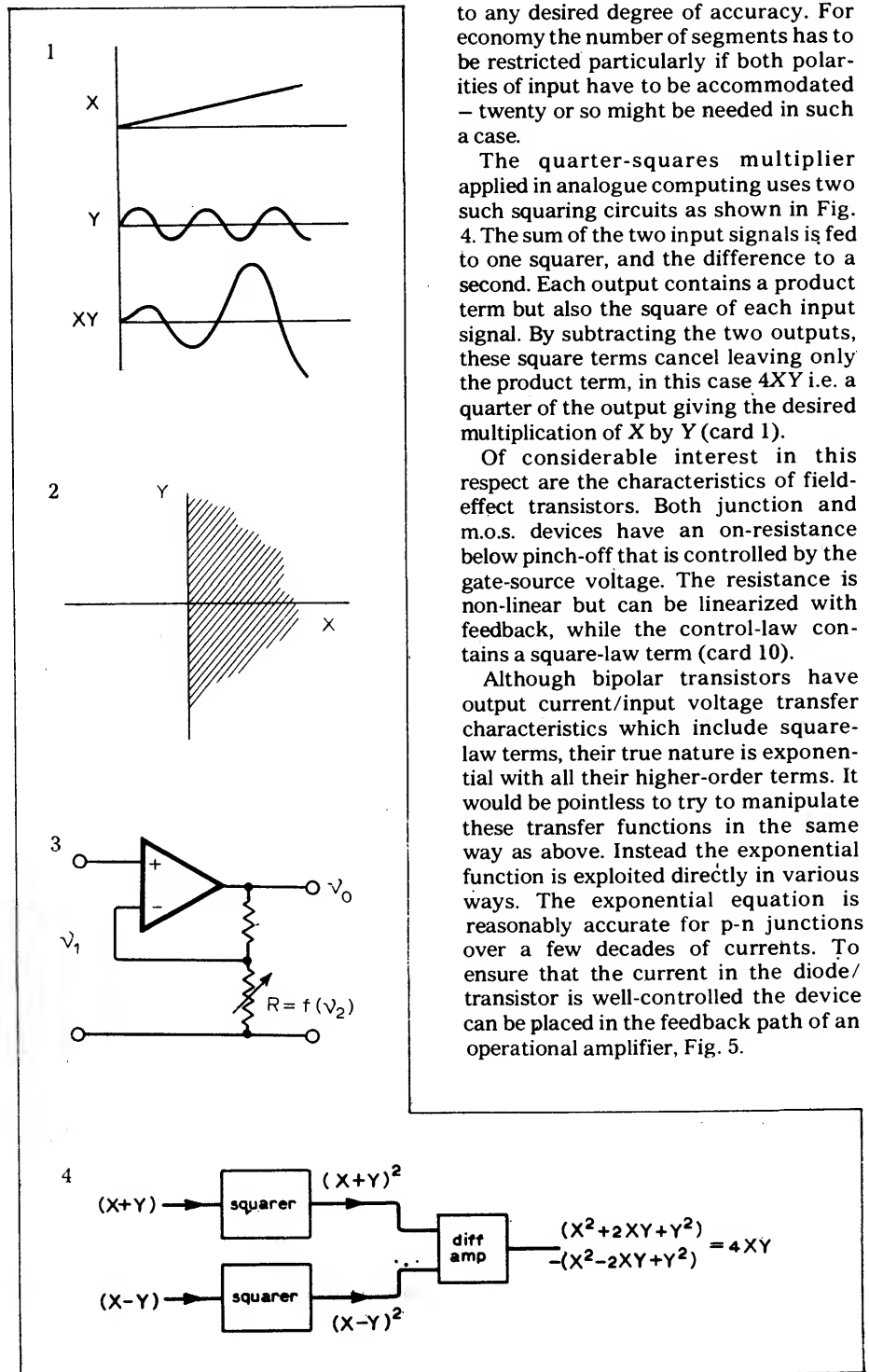
It can be very difficult to eliminate all unwanted terms consistently and over a wide range of temperatures and supply voltages. One well-established technique is to use a circuit with a square-law voltage transfer function. This can be synthesized by a "piece-wise linear" technique, where a network of diodes, resistors and reference voltages, provides a slope that changes progressively as the input increases (see card 1). With a large enough number of segments, a power law can be approached

to any desired degree of accuracy. For economy the number of segments has to be restricted particularly if both polarities of input have to be accommodated – twenty or so might be needed in such a case.

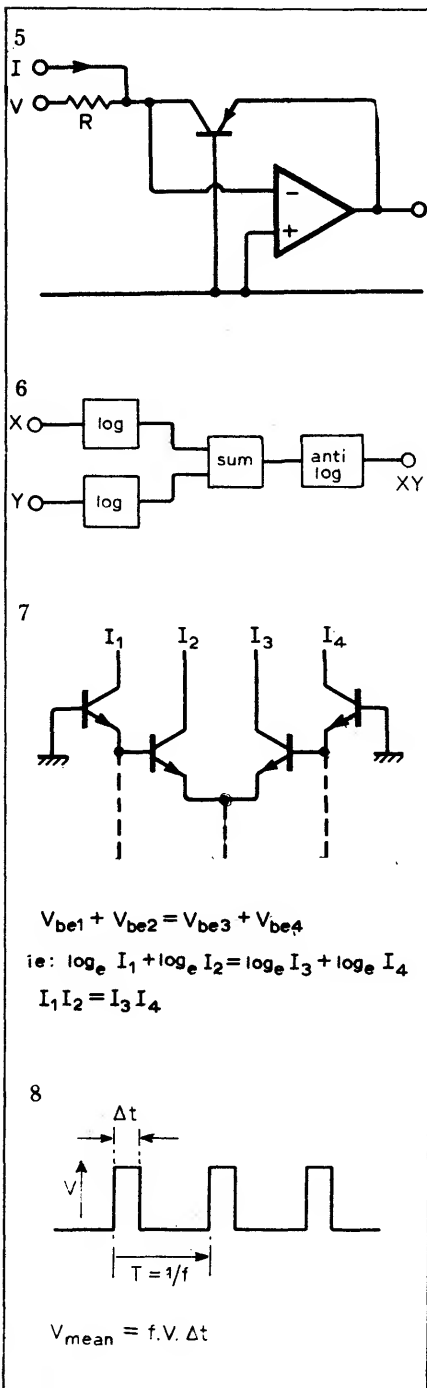
The quarter-squares multiplier applied in analogue computing uses two such squaring circuits as shown in Fig. 4. The sum of the two input signals is fed to one squarer, and the difference to a second. Each output contains a product term but also the square of each input signal. By subtracting the two outputs, these square terms cancel leaving only the product term, in this case  $4XY$  i.e. a quarter of the output giving the desired multiplication of  $X$  by  $Y$  (card 1).

Of considerable interest in this respect are the characteristics of field-effect transistors. Both junction and m.o.s. devices have an on-resistance below pinch-off that is controlled by the gate-source voltage. The resistance is non-linear but can be linearized with feedback, while the control-law contains a square-law term (card 10).

Although bipolar transistors have output current/input voltage transfer characteristics which include square-law terms, their true nature is exponential with all their higher-order terms. It would be pointless to try to manipulate these transfer functions in the same way as above. Instead the exponential function is exploited directly in various ways. The exponential equation is reasonably accurate for p-n junctions over a few decades of currents. To ensure that the current in the diode/transistor is well-controlled the device can be placed in the feedback path of an operational amplifier, Fig. 5.



One problem introduced by the use of a transistor is that of the increased loop gain, the transistor operating effectively in common-base with a voltage gain dependent on the input voltage. This leads to h.f. oscillation unless the amplitude-frequency response is carefully controlled by means of external compensation – one possibility being capacitive feedback from output to inverting input, by-passing the transistor at high frequencies. To use this logarithmic function for multiplication (as in card 4) the system shown in block diagram form in Fig. 6 may be used. The antilog circuit is simply a log circuit with input (resistor) and feedback (diode/transistor) elements interchanged. Similar systems can be devised to provide other power law and ratio circuits by expressing the desired function in log/antilog forms first.



A related technique uses multiple transistors (card 8), shown in a general configuration in Fig. 7. It is assumed that the currents are controlled by external generators and/or feedback with one of them, or the difference between two of them, as the output. In the example shown, for  $I_2$  maintained constant,  $I_1 \propto I_3 I_4$  i.e. a multiplier. As shown, operation would be restricted to a single quadrant, but a large number of circuits have been published both to extend the operation into all four quadrants and to produce a range of interrelationships such as those based on the log approach.

A totally different approach yielded many ingenious and effective multipliers, prior to the ready availability of matched transistors. It stems from the concept that the terms to be multiplied need not remain in the same physical domain while being processed e.g. the variables of interest may both be voltages and the output may also be required as a voltage but each input may be used separately to control a different parameter of an output waveform, while a third property might be proportional to the product of the other two.

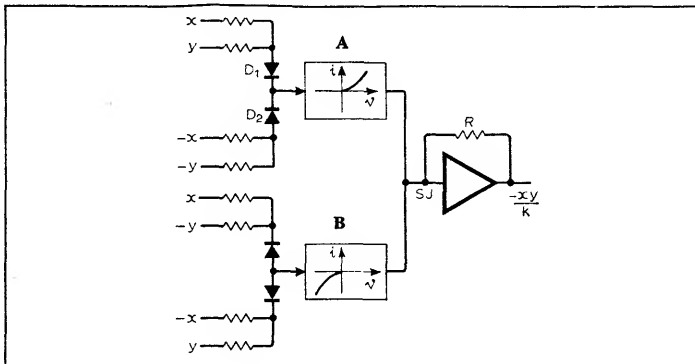
Consider the pulse waveform shown in Fig. 8. The pulse height is  $V$ , the repetition frequency  $f=1/T$  and the pulse width of  $\Delta t$ . The mean output voltage as would be indicated on a moving coil meter is given by the product of these three variables, increases in each individually producing a proportional change in that mean value. Thus if any pair of these variables ( $f, V$ ), ( $f, \Delta t$ ) or ( $V, \Delta t$ ) is brought under the separate and linear control of two input voltages, then the mean output voltage is a measure of the input product (card 2). There is a close relationship between these circuits and various forms of pulse modulators in the same way that the analogue multipliers described earlier are related to amplitude modulators.

There are purely digital methods of multiplication, but an intermediate solution is offered by the multiplying d.-to-a. converter. For a given binary input the converter has a number of output switches activated. If these operate on an external reference voltage the final output depends on the product of that reference voltage and the binary number. A class of digital circuits called binary-rate-multipliers is used to operate on a pulse train, producing a second train of pulses at a slower rate, card 3. At first sight this must cast doubts on the terminology since we associate multiplication with outputs greater than the inputs. The property of the circuit is however to multiply the input pulse rate by a factor such as  $n/100$  where  $n < 100$  and  $n$  can take up any value between 1 and 100, i.e. it is equivalent to multiplying by  $n$  but shifting the decimal point by two places.

The variety of methods available for achieving the multiplication of two

variables electronically is growing, and modules are readily available to a high degree of accuracy. As the methods vary widely in both properties and in the physical processes involved it is important to consider the options carefully – it is a field where the opportunities to place one's foot firmly in it (unspecified) are remarkably high.

**Quarter-squares multiplier**



**Description**

Quarter square multipliers are found frequently in analogue/hybrid computers in which their high accuracy (0.05% of half scale) is required and their limited bandwidth (less than 10kHz) is no disadvantage. They implement the relationship  $xy = \frac{1}{4}[(x+y)^2 - (x-y)^2]$  i.e. multiplication based on a square law device—this is usually a diode function generator permanently set to provide a square law action. Such generators are usually

single quadrant devices, e.g. A (above) requires a positive input and this necessitates the use of an absolute value circuit prior to it. If, for instance,  $(x+y)$  is positive then  $D_1$  conducts (and  $D_2$  does not) and a positive voltage is applied to A. Likewise if  $(x+y)$  is negative  $D_2$  conducts (and  $D_1$  does not) but again it is a positive voltage that is applied to A. Hence the output of A is proportional to  $|(x+y)|^2$ , which is the same as  $(x+y)^2$ . A similar argument applies to the other absolute value circuit, B; being a 3rd quadrant device, it produces a current proportional to  $-(x-y)^2$ .

The constant  $k$  appearing in the output expression depends on  $R$  and on the output characteristics of A and B. Generally, if the maximum value of  $X$  and  $Y$  is say  $P$  volts, then  $k$  is set to  $P$ . If an absolute value circuit does not precede the squaring section then a total of four squaring sections are necessary. Despite the apparent increased complexity this is still

sometimes done to avoid errors due to the diodes  $D_1$  and  $D_2$  and to provide further functions. An example of a square law generator circuit is shown (ref. 1). The current  $i$  has a total of 10 possible paths between P and the summing junction (SJ). Depending on the voltage at P, however, not all of these paths are open. If the voltage is very small, only one path, via the top R is open. With increasing voltage more paths become open so that the resistance between P and SJ decreases thus increasing the gain between P and the amplifier output in steps. The points at which these step changes in gain occur are termed breakpoints and are usually equally spaced as the figure above shows. Uniform breakpoint spacing allows identical slope increments and equal positive and negative errors. For this situation errors can be kept within  $x\%$  of half scale with  $10/\sqrt{x}$  segments. Unequal spacing of the break-points makes no significant difference to the overall accuracy although it is common to have one or two extra breakpoints near zero for improved accuracy.

The use of the diode string to provide some of the biasing functions provides temperature compensation as well. The capacitors shown increase the frequency response.

**Related circuits**

If bandwidth is not essential but increased accuracy is, then use can be made of the relationship  $m^2 = \frac{1}{4}(1 + 2u + u^2)$  where  $u = 2|m| - 1$ . The right hand side of this

equation is not totally dependent on  $u^2$  so that errors produced by a squaring circuit producing  $u^2$  have a reduced effect on the errors in  $m^2$ . One can, of course, invert the situation and say that, for the same accuracy, fewer breakpoints are necessary and a less expensive squarer is produced. A "card" mechanising the right hand side of the equation is simply inserted as the A card in the circuit overleaf and with minor modifications a B card is produced.

If we now examine

$$xy = \frac{x+y^2}{2} - \frac{x-y^2}{2} = m_1^2 - m_2^2$$

and apply the above equation for  $m$  we obtain

$$xy = \frac{1}{4}[2(u_1 - u_2) + (u_1^2 - u_2^2)] = \frac{1}{2}(|x+y| - |x-y|) + \frac{1}{4}(u_1^2 - u_2^2)$$

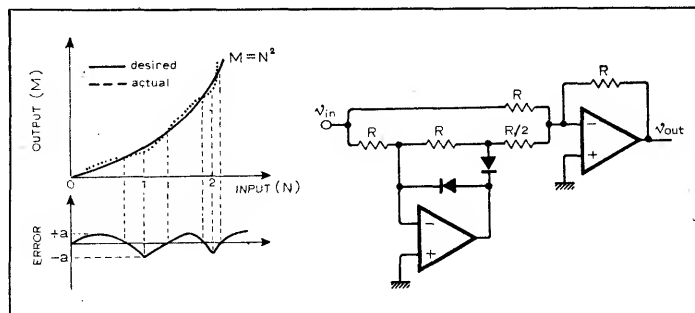
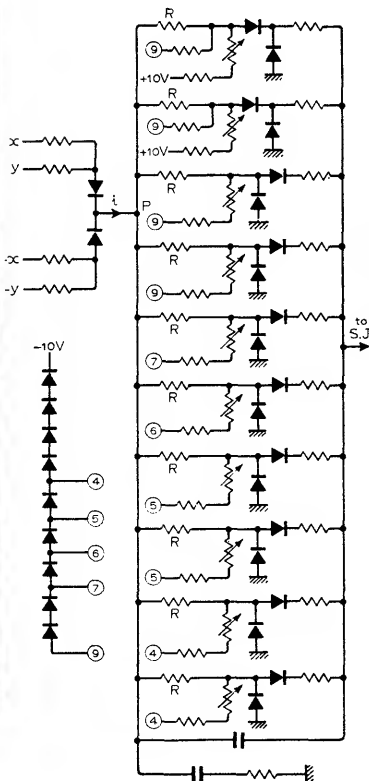
Reapplying the formula on the second bracketed term  $(u_1^2 - u_2^2)$  and truncating the series which will result from repeated application gives

$$xy \approx \frac{1}{2}(|x+y| - |x-y|) + \frac{1}{4}\{(|x+y| - 1) - (|x-y| - 1)\}$$

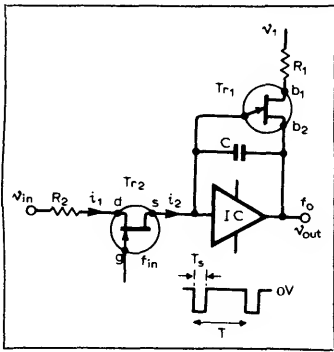
This does not require a squaring circuit and can be based on precision absolute value circuits such as those given in ref. 2

**References**

1. Whigham, R. H. Fast 10-V quarter-square multiplier. Simulation 1965.
2. Set 4, card 3. Korn and Korn. Electronic Analog and Hybrid Computers, 2nd edition, McGraw-Hill.



V-f converter multiplier



**Typical performance**  
 IC 741, ±15V supplies  
 Tr<sub>1</sub> 2N2646 u.j.t.  
 Tr<sub>2</sub> 2N5486 f.e.t. (n-channel)  
 R<sub>1</sub> 100Ω  
 R<sub>2</sub> 1kΩ  
 C 47nF  
 T<sub>s</sub> 100μs  
 Pulse height -5V

**Circuit description**

The circuit is a modification of the v-f converter described in ref. 1. The f.e.t. Tr<sub>2</sub> is the only addition. Graph 1 was obtained with f.e.t. permanently conducting, i.e. V<sub>gs</sub>=0 (f<sub>in</sub>=0), and shows f<sub>o</sub> to be proportional to v<sub>in</sub>. This graph was obtained with v<sub>1</sub> set to 3.3V which setting gave an f<sub>o</sub> of 2kHz with v<sub>in</sub>=2V. Control of the relationship between f<sub>o</sub> and v<sub>in</sub> depends on the u.j.t. breakdown voltage and this is variable from device to device.

The v-f conversion can be described as a conversion first from v<sub>in</sub> to i<sub>1</sub> and secondly from i<sub>1</sub> to f<sub>o</sub>. The greater i<sub>1</sub> the more rapidly does the capacitor charge and the more rapidly is the breakdown condition of the u.j.t. met. The downwards ramp of graph 2 shows this charging. On breakdown the u.j.t. shorts the capacitor so the output voltage rises towards zero until the u.j.t. assumes its normal non-conducting role.

If now pulses are fed to the f.e.t. gate as shown, i<sub>1</sub> will become a train of current pulses i<sub>2</sub>. f<sub>o</sub> then depends on i<sub>2</sub>.

$$f_o = k i_2 = k i_1 \cdot \frac{T_s}{T} = k \frac{v_{in}}{R_2} T_s \cdot f_{in} = k_1 v_{in} f_{in}$$

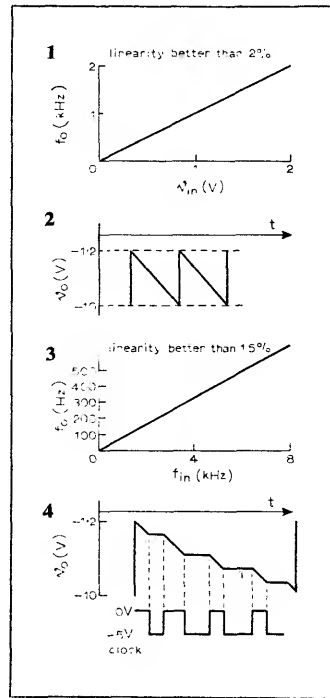
Graph 3 shows that f<sub>o</sub> is indeed proportional to f<sub>in</sub>, the proportionality between f<sub>o</sub> and v<sub>in</sub> being shown in graph 1. The multiplying action is thus experimentally verified.

If f<sub>in</sub> is derived from another v-f converter we have f<sub>in</sub>=k<sub>2</sub>v'<sub>in</sub> and then f<sub>o</sub>=k'' v<sub>in</sub> · v'<sub>in</sub> so that f<sub>o</sub> is proportional to the product of two voltages.

**Component changes.** The value of R<sub>2</sub> quoted i.e. 1kΩ is the absolute minimum usable. R<sub>2</sub> should be much larger than the f.e.t. "on" resistance (≈ 200Ω). Max. R<sub>2</sub> ≈ 100kΩ; beyond this op-amp input currents become significant. The value of C is related to that for R<sub>2</sub> as the ramp slope is 1/R<sub>2</sub>C. With C=4.7nF (and T<sub>s</sub>=10μs) we achieved a maximum f<sub>o</sub> of 10kHz. Higher values of f<sub>o</sub> are difficult to achieve because of charge-storage effects in the u.j.t. affecting the discharge time. Pulse height must be sufficient to cause pinch-off of f.e.t. but not so high as to cause breakdown. -1 to -10V with this device was satisfactory.

**Circuit modifications**

The circuit above shows a complete circuit whose output frequency, f<sub>o1</sub>, is proportional to the product of the voltages v<sub>1</sub> and v<sub>2</sub>. The second voltage to frequency converter, VFC<sub>2</sub>, is assumed to be identical to that shown in the main diagram overleaf with the omission of the f.e.t. gate; it will therefore produce an output as shown in graph 2. This output is fed to the c.m.o.s. monostable shown (ref. 2) in which V<sub>DD</sub>=0V and V<sub>SS</sub>=-10V (-15V would also be acceptable). This monostable is triggered when the c.p. voltage is about 50% of [V<sub>DD</sub>-V<sub>SS</sub>], the rising edge being the only one which is effective. The output pulse width is controlled by the R<sub>2</sub>C<sub>2</sub> time constant, resetting occurring when the voltage at R is approximately 50% of

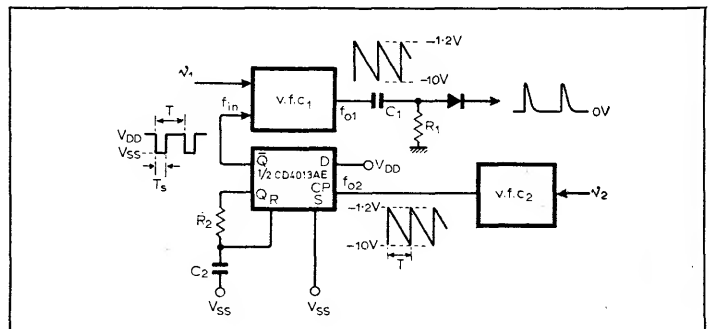


the input resistors and feedback capacitors will be different. Voltages v<sub>1</sub> and v<sub>2</sub> also affect the frequencies of operation. As the maximum frequency attainable from a unijunction type of v-f converter is of the order of 10kHz it may be necessary to use different types for a particular application. There is certainly no need for VFC<sub>1</sub> and VFC<sub>2</sub> to be of the same type. V-f converters have been considered in ref. 3. If different v-f converters are used different gating arrangements may well be required and in particular different monostables may be needed ref. 4. A multiplier using two identical (in form) v-f converters designed for long term stability and able to accommodate floating inputs is described in detail in ref. 5.

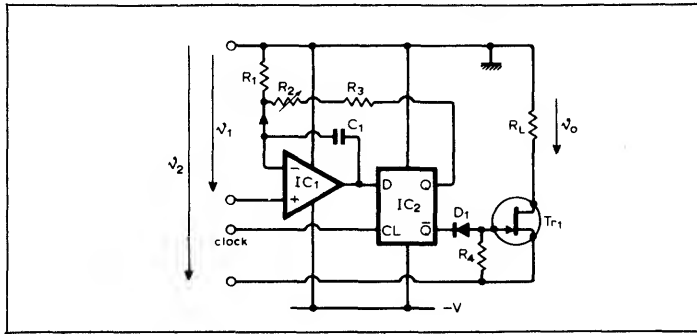
**Related circuits**

- 1 Set 21, V-f converters, card 1
- 2 Set 19, Monostables, card 8
- 3 Set 21, V-f converters
- 4 Set 19, Monostables
- 5 Versatile integrator-multiplier, E. Ljung and S. Berglund, *Electronic Engineering*, Aug. 1974, pp. 38-40.

[V<sub>DD</sub>-V<sub>SS</sub>]. Taking the output from Q gives trigger pulses of the correct polarity to gate the f.e.t. in the input path of VFC<sub>1</sub> which is identical to that shown. The output f<sub>o1</sub> will then be as shown in graph 4. The network comprising C<sub>1</sub>, R<sub>1</sub> and D<sub>1</sub> is simply a differentiating network to produce a somewhat more normal type of pulse train. Note that f<sub>in</sub> is equal to f<sub>o2</sub> and that f<sub>o1</sub> must be less than f<sub>in</sub>. In fact consideration of the operation of the system overleaf shows that f<sub>in</sub> should be of the order of ten times the desired f<sub>o1</sub>. Hence VFC<sub>2</sub> must operate at a much higher frequency than VFC<sub>1</sub> and consequently



## Delta-sigma modulator/multiplier



## Circuit description

If an output waveform has a constant pulse height and width but the pulse-rate is proportional to an input voltage, then the mean value of the output is also proportional to that voltage. If the pulse height is made proportional to a second voltage the mean output becomes proportional to the product of the two voltages. A delta-sigma modulator converts a pulse-train into one with a smaller number of pulses, using an integrator to control the voltage on the D input of a flip-flop. As the mean voltage at the inverting and non-inverting inputs are the same and the mean current in the capacitor is zero, the fraction of the time for which Q is high is controlled by the input voltage  $v_1$ . The circuit configuration has a negative input voltage and supply because it was desired to use the simplest arrangement, and certain op-amps (e.g. Signetics 741) have an input common-mode range that includes the positive supply rail. The circuit can be adapted for any other op-amp by providing a separate positive bias. With dual supplies the system may equally be used with positive inputs and outputs if the flip-flop is powered from the positive rail.

The Q output is used to gate a junction f.e.t. on and off. With Q high (zero volts), the diode is non-conducting and  $R_4$  establishes zero gate-source bias. With Q low ( $-V$ ) the f.e.t. is off. This is true provided the second input

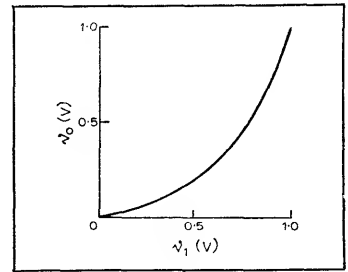
voltage  $v_2$  is small so that the reverse gate-source voltage is in excess of the pinch-off voltage. The load receives voltage pulses of duration equal to the inter pulse period and just less than  $v_2$  in magnitude. The number of pulses in a given time is proportional to  $v_1$ . Hence the mean load voltage is  $\propto v_1 v_2$ . This can be read directly on a moving-coil meter, or filtered and fed to a d.v.m.

## Component changes

**IC<sub>1</sub>:** Any op-amp if supply requirements observed. Output is always close to the flip-flop threshold voltage i.e. does not approach either supply line. Supplies can be single-ended negative or positive depending on op-amp. Must be large enough to gate f.e.t. 6 to 15V.  
**Tr<sub>1</sub>:** Any n-channel junction f.e.t. with pinch-off below, say, 5V. Low on-resistance preferred.  
**D<sub>1</sub>:** General purpose switching diode.  
**IC<sub>2</sub>:** Any c.m.o.s. D-type flip-flop (set and reset grounded).  
**R<sub>1</sub>, R<sub>2</sub>, R<sub>3</sub>:** Ratio sets 'gain' i.e. usual potential divider

## Typical performance

IC<sub>1</sub> N5741V (Signetics)  
 IC<sub>2</sub>  $\frac{1}{2}$ CD4013  
 D<sub>1</sub> 1N4148  
 Tr<sub>1</sub> 2N5457  
 R<sub>1</sub> 4.7k $\Omega$   
 R<sub>2</sub> 100k $\Omega$  pot.  
 R<sub>3</sub> 100k $\Omega$   
 R<sub>4</sub> 15k $\Omega$   
 R<sub>L</sub> 15k $\Omega$   
 Supply  $-10V$   
 $v_1, v_2$  0  $\rightarrow$   $-1V$   
 $v_0$  0  $\rightarrow$   $-1V$   
 $|v_0| = v_1 v_2$



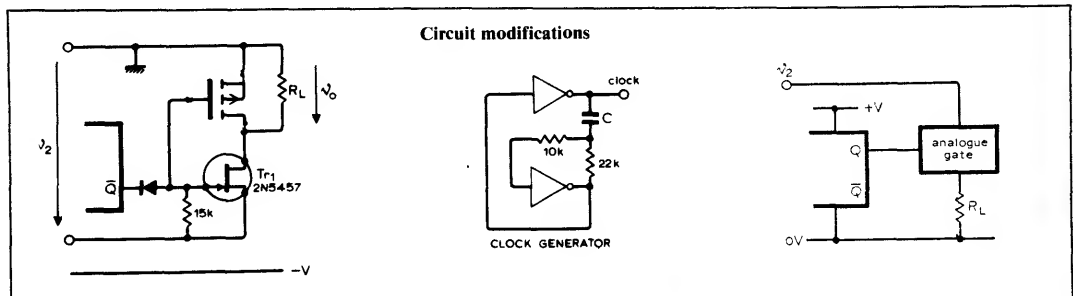
relationship defines ratio of mean output at Q to  $v_1$ . Total resistance 10k to 10M $\Omega$ . Suggested ratios 5: 1 to 20: 1. **R<sub>4</sub>:** If too high, results in slow switching of f.e.t. from off-on state with reduced overall accuracy. If too low, additional current places unwanted extra load on  $v_2$  source.  
 $v_1, v_2$ : Typically 0  $\rightarrow$   $-1V$ .  $v_1$  feeds into very high impedance,  $v_2$  has to supply load current via Tr<sub>1</sub>.  
**R<sub>L</sub>:** Compromise between sensitivity of meter and loading of  $v_2$  5k to 50k $\Omega$ .

## Circuit modifications

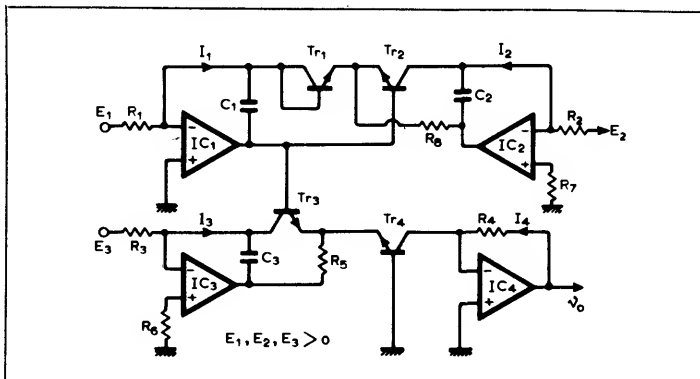
● To improve switching times without adding an extra i.c., it is possible to use a p.m.o.s. transistor from a CD4007 package. If the remainder of the package is connected as in the circuit shown, a clock generator results. Frequencies from 10kHz to  $>100kHz$  have been tested with this system. In general clock rates of several MHz are feasible but would make heavy demands on the analogue switches. The p.m.o.s. device prevents charge storage

across the load resistance in the off-state, and allows the high load resistance represented by a d.v.m. to be used. This makes the input impedance at the  $v_2$  input high, without restricting the switching rate.

- If positive input voltages are used, and standard analogue gates are available, then a series switch arrangement as shown may be driven from the Q output. Then when  $v_1$  is at its maximum value, Q is almost permanently at logic 1 and  $v_2$  is gated through to the load for almost 100% of the time. A shunt gate driven from Q completes the configuration for higher switching speeds or where  $R_L$  is to be raised.
- In principle this can be interpreted as a combined  $V_1$ -f and  $V_2$ -amplitude converter system.

Related circuits  
Set 15, card 9

Log-antilog multiplier



Components

IC<sub>1-4</sub> 741 (e.g. RC4136 quad package)

Tr<sub>1</sub> to Tr<sub>4</sub> 1/5 CA3086

R<sub>1</sub>, R<sub>2</sub>, R<sub>3</sub>, R<sub>6</sub>, R<sub>7</sub> 100kΩ

R<sub>4</sub> 10kΩ, R<sub>5</sub> 2.2kΩ

C<sub>1</sub> 300pF, C<sub>2</sub> 200pF

C<sub>3</sub> 22pF

All passive components ±5%

Supply voltage ±7.5V

Performance

It can be shown (see text) that  $v_o = E_1 E_3 R_2 R_4 / E_2 R_1 R_3$ . With the resistor values chosen, assuming perfect components,  $v_o = E_1 E_3 / 10 E_2$  and so the circuit can be used as a squarer ( $E_1 = E_3$  and  $E_2$  constant), as a multiplier ( $E_2$  constant  $E_1$  and  $E_3$  variable), as a divider ( $E_2$  as divisor  $E_1$  or  $E_3$  as dividend, the other fixed) or as a device for obtaining the reciprocal of  $E_2$  ( $E_1$  and  $E_3$  fixed). Results as a squarer are shown in graph 1 from which it will be noted that  $E_2$  was set at 0.92 rather than 1V to achieve the slope of 45°

(making up for component inaccuracy) and that the maximum  $v_o$  obtainable is less than 4V. Saturation of the transistors occurs at higher voltages. Graph 2 shows similar linearity for operation as a multiplier, multiplying the variable  $E_1$  by the constant  $E_3$ . Identical results were obtained when the roles of  $E_1$  and  $E_3$  were reversed. Similar linearity was obtained with the device operated as an arithmetic inverter (reciprocal).

Circuit description

Analysis of the circuit is as follows:

$$I_1 = E_1 / R_1 \text{ and } V_{be1} = \frac{kT}{q} \log_e I_1$$

$$I_2 = E_2 / R_2 \text{ and } V_{be2} = \frac{kT}{q} \log_e I_2$$

$$V' = V_{be2} - V_{be1} = \frac{kT}{q} \log_e \frac{E_2 R_1}{E_1 R_2}$$

$$V_{be4} = -V' + V_{be3} = -\frac{kT}{q} \log_e \frac{E_1 E_3 R_2}{E_2 R_1 R_3} \quad (1)$$

$$\text{as } V_{be3} = \frac{kT}{q} \log_e I_3 \text{ and } I_3 = E_3 / R_3.$$

But  $\log_e I_4 = q V_{be4} / kT$  and

$$I_4 = V_o / R_4$$

Combining this last pair of equations with equation 1 gives

$$V_o = \frac{E_1}{E_2} E_3 \frac{R_4 R_2}{R_3 R_1}$$

A functional block diagram following from these equations is shown, right. The antilog function is performed by Tr<sub>4</sub> and IC<sub>4</sub>. Principally it is Tr<sub>4</sub> which performs the antilog function in converting its base-emitter voltage to a current: IC<sub>4</sub> and R<sub>4</sub> convert

this current to a voltage, viz  $V_o$ .

The above analysis concerned d.c. conditions only, so all capacitors were ignored. Likewise R<sub>5</sub> and R<sub>8</sub> were ignored. The function of all of these components is to stabilize the loops in which they are contained. To see this, consider the simplest case viz IC<sub>3</sub> and its associated circuitry. The loop gain of this circuit is the open-loop gain of IC<sub>3</sub> together with the gain of Tr<sub>3</sub> which is in common base mode and has a voltage gain given

approximately by  $g_m \times$  the load on Tr<sub>3</sub>. The load on Tr<sub>3</sub> is R<sub>3</sub> (by superposition the E<sub>3</sub> input end of R<sub>3</sub> is at ground). This voltage gain  $g_m R_3$  is large and the overall loop gain is, therefore, considerably enhanced and instability is a considerable problem. The inclusion of R<sub>5</sub> reduces the feedback path gain as only a portion of the i.c. output voltage is applied to the base-emitter junction. For high frequency effects C<sub>3</sub> completely shorts out this feedback path amplifier, again improving stability. Note that  $g_m$  depends on the operating conditions i.e., in this case, on E<sub>3</sub> so that the problem is complex indeed. Note that all the input voltages must be positive to maintain correct transistor biasing. If a sinusoid is to be used it must be suitably biased to prevent negative going inputs and the output circuitry must be considerably rearranged to remove the effect of the biasing term on the output.

a much tighter tolerance.

Nulling of i.c.s will improve performance as will the use of i.c.s with facility for feedforward compensation e.g. LM301 etc. The use of i.c.s with very low input currents e.g. LM108 or f.e.t. input i.c.s such as CA3130 will improve the lower end of the input range. These comments do not apply strictly to IC<sub>4</sub> which simply converts the current through Tr<sub>4</sub> to a voltage. Indeed, an appropriate moving coil meter connected between the collector of Tr<sub>4</sub> and ground will suffice to give a reading of the output.

Further reading

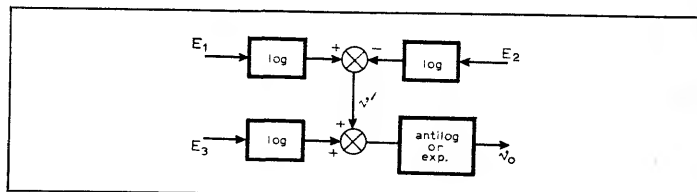
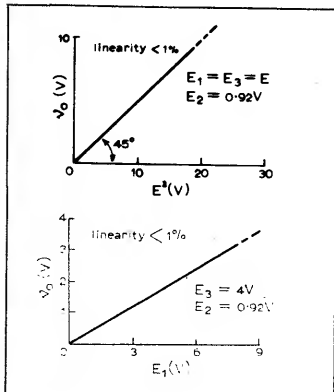
National Semiconductor application notes AN-30.

Related circuits

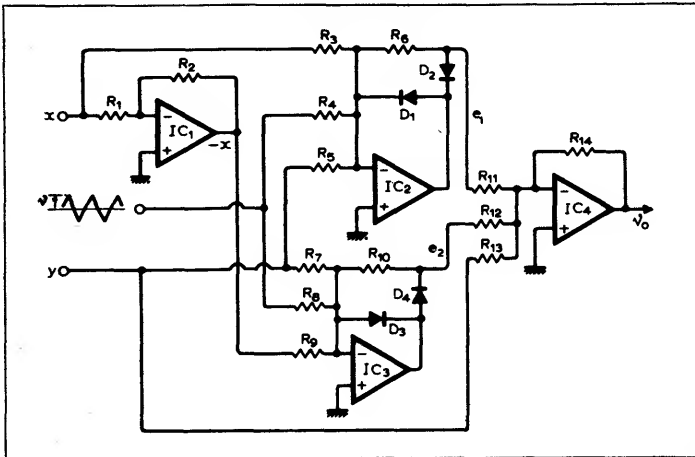
Set 4, card 11

Component changes

This circuit was built from the cheapest possible components and no effort was made to null the i.c.s. Considerable improvement in accuracy is obtainable if the resistors R<sub>1</sub>R<sub>2</sub>R<sub>3</sub> and R<sub>4</sub> are chosen to



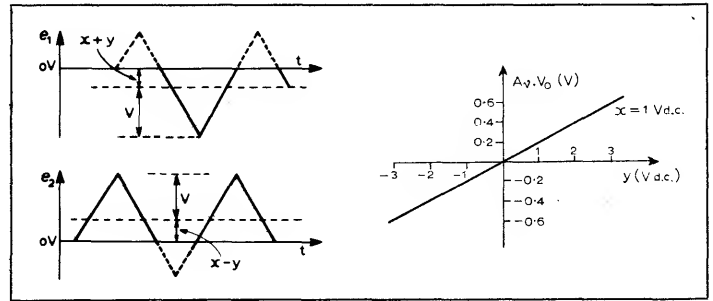
**Triangle-wave averaging multiplier**



**Components**  
 R<sub>1</sub> to R<sub>14</sub> 120kΩ  
 IC<sub>1</sub> 741  
 D<sub>1</sub> 1N914  
 Supplies ±15V

**Performance**  
 With v set at 4V and the

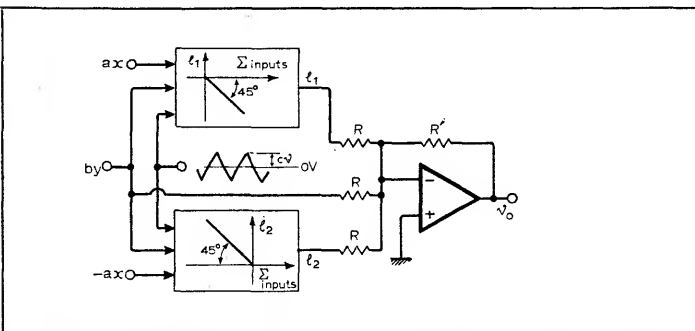
frequency of the triangular waveform set at 1kHz graphs 1 and 2 were obtained. Linearity shown in graph 2 is better than 1%. Note that x and y are direct voltages and v<sub>o</sub> is the average voltage at the output of IC<sub>4</sub>. v<sub>o</sub> is, of course, the



inverted sum of e<sub>1</sub>, e<sub>2</sub> and y. With x and y both at 1V and varying the frequency of the triangular wave the output accuracy was maintained within 1% up to 6kHz. The device is a 4-quadrant multiplier.

**Description**  
 The block comprising IC<sub>2</sub>, R<sub>3</sub>, R<sub>4</sub>, R<sub>5</sub>, R<sub>6</sub>, D<sub>1</sub> and D<sub>2</sub> is a precision half-wave rectifier producing a negative output equal in magnitude to the sum of the input voltages when that

sum is positive. The block producing e<sub>2</sub> can likewise be described. The sum of e<sub>2</sub>, e<sub>1</sub> and y produces the output and at first sight the multiplier appears related to time-division (a.m./p.w.m.) multipliers. Analysis shows however that this multiplier is more closely related to the quarter-square multiplier, the reason being that the height of e<sub>2</sub> is closely related to the base of hatched triangle in graph 1 so that the area of the triangle becomes a square function.



A more general diagram is shown above: for this system it can be shown that the average value of V<sub>o</sub> is:

$$-\frac{R'}{R} (\text{average of } e_1 + \text{average of } e_2 + by)$$

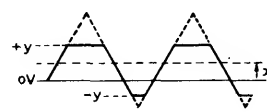
$$= -\frac{R'}{R} \left[ \frac{-1}{4cV} (cV + ax + by)^2 + \frac{1}{4cV} (cV + ax - by)^2 + by \right]$$

If R' = αR, then this expression simplifies to

$$V_{oav} = \alpha xy \frac{ab}{cV}$$

Comparing this with the circuit overleaf we see that we have α = a = b = 1 and cV = 4.

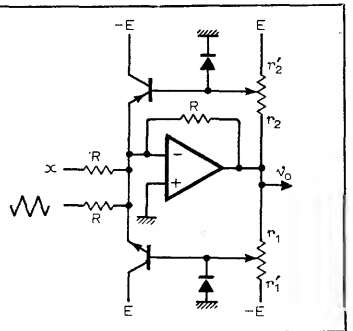
Returning now to the original circuit one can observe that the somewhat restricted input range is due to the fact that at no point should the bias voltage exceed the peak of the triangular wave. Clearly the input signal size can be increased by increasing the carrier magnitude and also by introducing factors a and b, reducing the effective input. The effect of these changes can be then cancelled by setting R' = α cV/ab. The circuit is sensitive to d.c. components in the carrier and also to the carrier magnitude. The effect of a d.c. component



is particularly noticeable at low signal levels.

**Circuit modifications**  
 Resistor values are not critical but lower values than those shown may be preferable to improve the bandwidth by reducing the time constants of stray and other capacitive paths. Resistor R' may be replaced by a filter to remove the a.c. components of V<sub>o</sub>. The d.c. impedance of such a filter should still equal R'. The system bandwidth can be increased by using a faster version of half-wave rectifiers<sup>1</sup>.

- An alternative scheme is

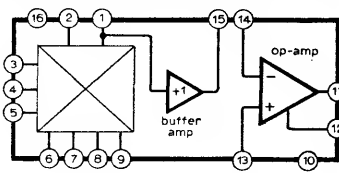


shown above; this arises from the fact that the product xy is obtained by biasing a triangular wave by x and limiting the resultant at ±y. A suitable high speed limiter is shown above. The output is limited at r<sub>1</sub>E/r' for negative inputs and at -r<sub>2</sub>E/r<sub>2</sub>' for positive inputs. These would be set to ±y respectively. Note that r<sub>1</sub> r<sub>2</sub> ≪ R for good limiting.

**References**  
 1 Set 22, card 3  
 2 Korn & Korn, Electronic Analog and Hybrid Computers, 2nd edition McGraw-Hill.



### Four-quadrant multiplier—characteristics



#### Pin designation

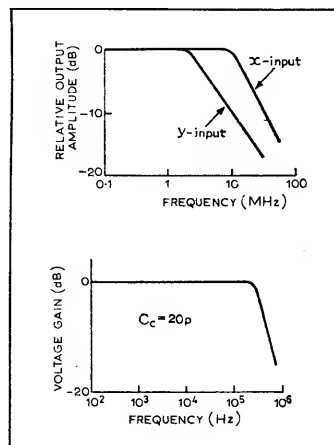
1, 2 multiplier outputs	11 op-amp output
3 x input 4 common	12 compensation
5 y input 6 and 7 y gain	13 non-inverting op-amp input
8 and 9 x gain	14 inverting op-amp input
10 negative supply	15 high-frequency output
	16 positive supply

#### Description

The XR-2208/2308 is an op-amp combining a four-quadrant analogue multiplier, a high-frequency buffer amplifier and a differential-input op-amp on the same monolithic integrated circuit. The package is suitable for arithmetic operations and communication signal processing, maximum versatility being achieved by internally separating the amplifier and the multiplier-buffer section; suitable interconnections being made externally with passive components. The op-amp can be used as a post-detection amplifier in coherent detector applications or as a preamplifier for low-level input signals. The output from the buffer amplifier can be used for high-frequency signal processing, the multiplier-buffer section having a small-signal 3dB bandwidth of 8MHz and a transconductance bandwidth of 100MHz.

The package can be operated from symmetrical supply rails in the range  $\pm 4.5$  to  $\pm 16$ V. Very good power supply rejection and temperature stability are achieved by internally-regulating current and voltage levels.

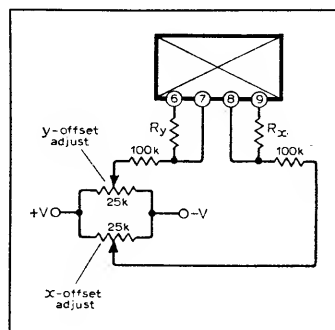
The multiplier inputs x and y are applied to pins 3 and 5 respectively, with pin 4 common—normally the reference or ground terminal. However, in some applications x and y inputs are strapped together and pin 4 used as an



input terminal. The d.c. bias currents at pins 3 and 5 are typically  $3\mu\text{A}$  and at pin 4 typically  $6\mu\text{A}$ . The differential output voltage ( $v_o$ ) between pins 1 and 2 is often connected directly to the op-amp (pins 13 and 14), the final output ( $v_z$ ) being obtained from pin 11.

$$v_o \approx \frac{25}{R_X \cdot R_Y} v_X \cdot v_Y$$

where all voltages are in volts and the gain control resistances



( $R_X$  and  $R_Y$ ) for the x and y sections of the multiplier are in  $k\Omega$ . Conversion gain of the multiplier is

$$K_M \approx \frac{25}{R_X \cdot R_Y} (V-1)$$

resistors  $R_X$  and  $R_Y$  being connected as below, where the arrangement for adjusting the x and y offsets at pins 7 and 8 is also shown.

The operational amplifier is internally protected against short-circuit load conditions and can sink or source a current of 10mA into a resistive load. This amplifier can be compensated for unconditional stability by connecting a capacitor ( $C_C$ ) of 20pF across pins 11 and 12. For higher voltage gains than unity,  $C_C$  is reduced to increase small-signal bandwidth and to improve slew-rate.

The unity-gain buffer amplifier if brought into use by connecting a resistor from pin 15 to ground and provides a low-impedance output for the multiplier section when the latter is used at high frequencies, in order to minimize capacitive loading of the multiplier output proper. The buffer output is not short-circuit protected and typically has a direct voltage of  $V^+ - 4.5$  volts. The maximum direct current extracted from pin 15 should not exceed 10mA. NOTE: When only the multiplier section or op-amp section is being used the input terminals of the unused section must be connected to ground. The maximum peak x or y input signal that can be used for a given supply voltage without significant improvement of the linearity of the multiplier is shown.

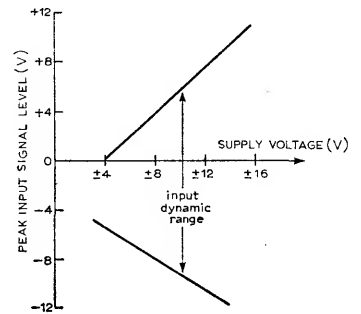
#### Further reading

XR-2208/2308 Operational multiplier data sheet, EXAR, 1972.

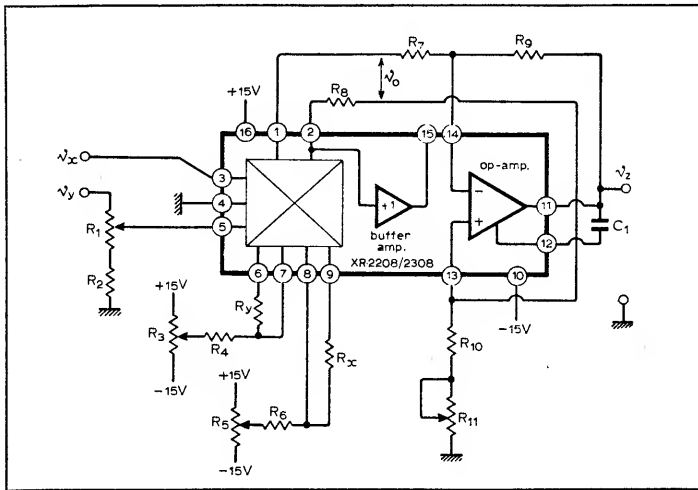
XR-2208 Operational Multiplier, *New Electronics*, 1 April 1975, pp. 27-31.

#### Related circuits

Set 29, card 7



**Four-quadrant multiplier—applications**



**Component values**

- Supplies  $\pm 15V$
- $V_{x(max)}, V_{y(max)}$  10V
- $R_1, R_2$  5k $\Omega$
- $R_3, R_4, R_5, R_6, R_{11}$  100k $\Omega$
- $R_7, R_8$  24k $\Omega$ ,  $R_9$  300k $\Omega$
- $R_{10}$  240k $\Omega$ ,  $R_x$  30k $\Omega$
- $R_y$  62k $\Omega$ ,  $C_1$  20pF
- $V_z = V_x \cdot V_y / 10$
- $R_1$  scale factor
- $R_3$  y-offset
- $R_5$  x-offset
- $R_{11}$  output offset

means of the 25k $\Omega$  potentiometer which sets the d.c. level at pin 3. In suppressed-carrier applications, the carrier level at the output can be further reduced by means of the x and y offset adjustment controls. The buffer amplifier provides a unity gain low-impedance output, but if not required pin 15 should be open circuited to reduce power dissipation. Carrier suppression of 40dB up to 1MHz and 30dB up to 10MHz is obtainable without the use of the x and y offset adjustments.

**4-quadrant multiplier—applications**

In most multiplication applications the operational amplifier and multiplier sections are interconnected as shown left providing a single-ended output signal and having a wide dynamic range. With the values shown below, the linear output swing is typically 10V for maximum input signals of 10V with a scale factor  $K=0.1$ .

1. With 0V applied to the input and 0V to the x-input and 0V to the y-input,  $R_5$  is adjusted to provide minimum output voltage.
2. Repeat step 1.
3. With +10V applied to both inputs,  $R_1$  is adjusted to provide an output of +10V.
4. Step 3 may be repeated with different input voltages and different polarities to obtain best accuracy either over the whole input range or over some specific part of it.

1. With 0V applied to the input the output offset is adjusted to be 0V using  $R_{11}$ .
2. With +1V applied to the input  $R_3$  is adjusted to make  $v_o$  0.1V.
3. With +10V applied to the input the output is adjusted to be +10V using  $R_1$ .
4. With -10V applied to the input check that the output is +10V, if this is not so repeat steps 1 to 3.

**Synchronous a.m. detector**

The circuit (right) is suitable for demodulation of a.m. signals with carrier frequencies up to 100MHz, with an input signal of at least 25mV r.m.s. The a.m. input is applied to the common terminal of the multiplier, the y-gain terminals are strapped allowing this section to act as a limiter for inputs greater than about 50mV r.m.s. and the x-section acts in its linear mode. Capacitors  $C_1$  at pins 1 and 2 in the low-pass filter serve to reduce the carrier feedthrough to the output.

**Setting-up procedure**

- 1 With 0V applied to both inputs the output offset is adjusted to be 0V with  $R_{11}$ .
- 2 With a 20V pk-pk, 50Hz signal applied to the x-input and 0V to the y-input,  $R_3$  is adjusted to provide minimum output voltage.
- 3 With a 20V pk-pk 50Hz

**Squaring circuit**

As shown over, the circuit used for squaring is essentially that used for multiplication except that the input signal is applied simultaneously to the x and y input terminals and only one input offset adjustment is required. Adjustment procedure is:

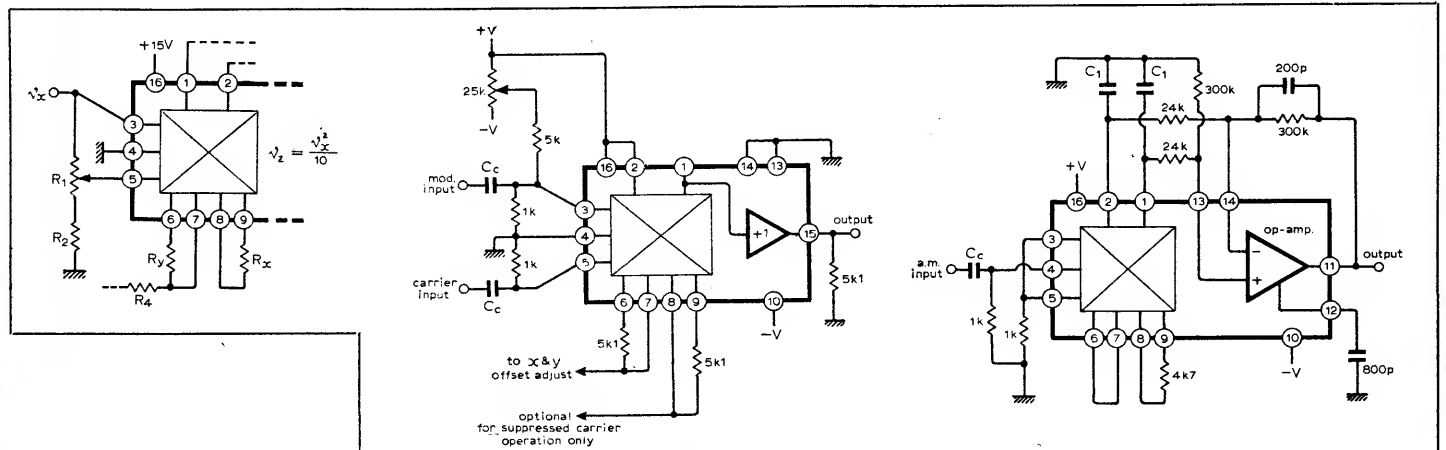
**A.m. generator**

The circuit (middle) is that recommended for generating double sideband signals or for suppressed-carrier a.m. generation. Modulation and carrier are applied to the x and y inputs respectively with a carrier level of 1V (r.m.s.). The level of the carrier appearing at the output is adjusted by

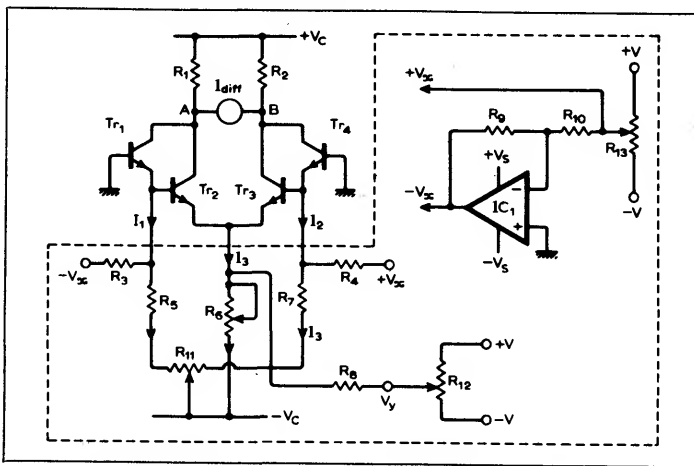
**Further reading**

XR-2208/2308 Operational multiplier data sheet, EXAR, 1972.

**Related circuits**  
Set 29, card 6

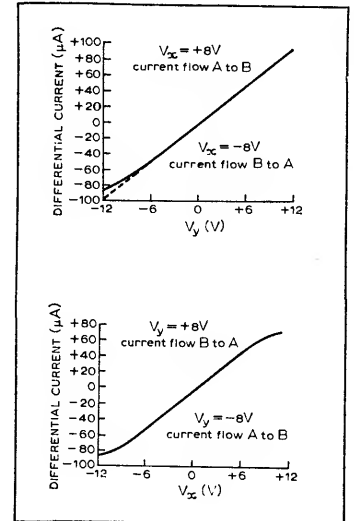


**Translinear multiplier**



**Typical data**

Tr<sub>1-4</sub> 1/5 CA3086  
 R<sub>1</sub> 47kΩ ±5%  
 R<sub>2</sub> 46.6kΩ (trimming required)  
 R<sub>3, R4, R5, R7, R8</sub> 100kΩ ±5%  
 R<sub>6</sub> 68.7kΩ (trimmed)  
 R<sub>9, R10</sub> 50kΩ IC<sub>1</sub> 741  
 R<sub>11</sub> 100kΩ R<sub>12, R13</sub> 10kΩ  
 V<sub>c</sub> ±15V  
 V: ±12V V<sub>s</sub>: ±15V  
 N.B. Pin 13 of CA3086 must be connected to most negative potential.



**Circuit description**

The circuit currents above are related to a defined current unit I, by the following:  
 $I_1 = (1 + X)I/2$   $I_2 = (1 - X)I/2$   
 $I_3 = (1 + Y)I$   
 where X and Y are controlled variables, and I<sub>diff</sub> between Tr<sub>2</sub> and Tr<sub>3</sub> collectors is  $XYI$ . The circuit operates in the current domain and depends for its temperature independence on the proportionality of bipolar transistor g<sub>m</sub> (transconductance) to the collector current. Currents I<sub>1</sub>, I<sub>2</sub>, I<sub>3</sub> are ideally current sources, and the above network comprising V<sub>x</sub>, V<sub>y</sub>, resistors R<sub>3</sub> to R<sub>7</sub> is an attempt to simulate such a condition e.g. I<sub>3</sub> is approximately equal to  $-V_c/(R_7 + R_{11}/2) \approx 100\mu A$  plus

a multiple of 100μA defined by  $V_x/R_4$  where V<sub>x</sub> is increased in steps of 1V. These calculations assume that the base-emitter junction voltages are negligible. To obtain a balanced condition where I<sub>diff</sub>=0 if either V<sub>x</sub> or V<sub>y</sub> is zero demands trimming of resistor R<sub>6</sub> and R<sub>2</sub> to allow for the 1.2V potential at the emitters of Tr<sub>2</sub>, Tr<sub>3</sub>. Linearity of I<sub>diff</sub> is shown in accompanying graphs. Note, that if V<sub>x</sub>=+8V, this is equivalent to eight units of current, and if V<sub>y</sub>=+2V, two units of current. Resulting product is 16.

**Parameter changes**

If X=Y, the output function is a squared function of those variables. Graphs of the

resulting current variation are given above. For each graph, the effect of Y being negative causes a slight deviation from the true square law. Possibly due to inexact compensation for V<sub>BE</sub> drops with network employed.

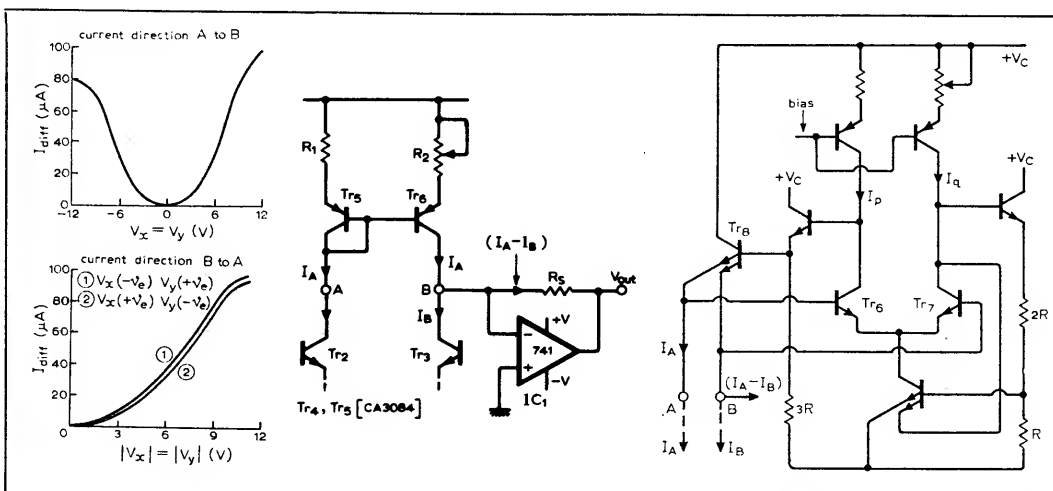
**Component changes**

Circuit is supply sensitive, especially at the low levels of current I. At V<sub>c</sub>=±15V, a 20% reduction of V<sub>c</sub> provides a -3% error for I<sub>diff</sub>=81μA, but at 9μA, +30% error.

**Circuit modifications**

- Use of transistors Tr<sub>4</sub>, Tr<sub>5</sub> in a current mirror configuration will permit the differential current to be obtained with respect to ground. R<sub>1</sub> and R<sub>2</sub> are adjusted to be

similar to obtain equal collector currents in Tr<sub>4</sub>, Tr<sub>5</sub>. This current is converted to an equivalent voltage by driving into IC<sub>1</sub>, such that  $V_{out} = -(I_A - I_B)R_s$ . A more sophisticated technique<sup>2</sup>, with a wide frequency response, is shown extreme right. Transistor Tr<sub>8</sub>, which has a double emitter, could be derived from a monolithic package by paralleling collectors and bases. The bias voltage which should be the silicon bandgap voltage (1.205V) minimizes the current ratio I<sub>p</sub>/I<sub>q</sub> drift with temperature. If I<sub>p</sub>=I<sub>q</sub>, then the base-emitter junction voltages of Tr<sub>6</sub> and Tr<sub>7</sub> are equal (for equal emitter areas). This implies that the emitters of Tr<sub>8</sub> are at the same potential, and hence the currents are equal.

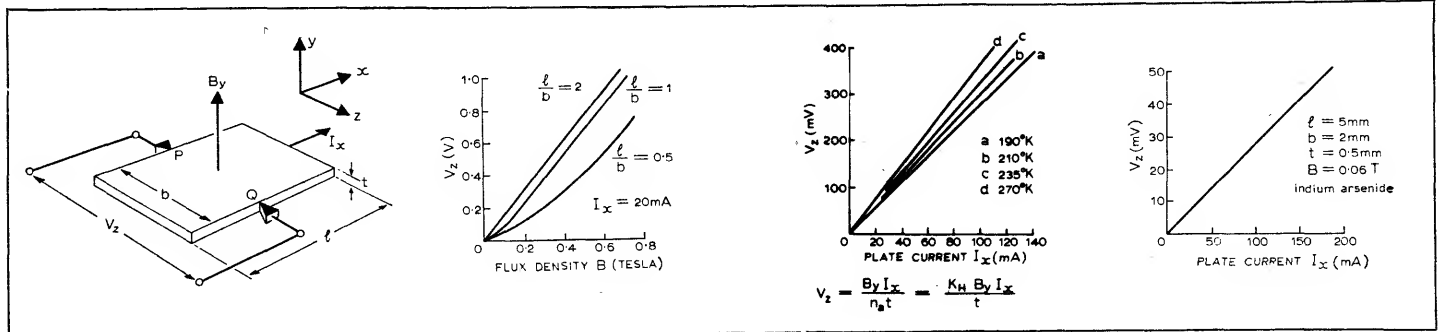


**Further reading**

- 1 Gilbert, B. Translinear circuits: A proposed classification, *Electronics Letters*, 9 Jan. 1975. vol. 11, no. 1.
- 2 Gilbert, B. Wideband negative current mirror, *Electronics Letters*, 20 March, 1975. vol. 11, no. 6.
- 3 Korn & Korn. Electronic analogue and hybrid computers. McGraw Hill 1972.

**Related circuits**

- Set 6, card 4
- Set 23, card 5



**Hall-effect multiplier**

**Hall-effect multiplier**

In a practical Hall plate, point electrodes between which the Hall voltage is developed are connected midway between the end-electrodes. Materials used for the plate are high mobility bulk semiconductors, with low conductivity: indium arsenide, germanium, indium antimonide.

**Background**

The device produces an output voltage dependent on the product of two inputs—the plate current  $I_x$ , and an external magnetic field  $B_y$  (Tesla). Current flow is due to electrons  $n$ , charge  $q$  and drift velocity  $v_x$ . Hence current density

$$J_x = I_x / bt = nqv_x$$

Deflecting force on electrons in direction Z due to  $B_y$  is

$$F_z = B_y qv_x$$

At equilibrium, this just balances the field force due to electron deflection, i.e.  $qE_z$ ,  $B_y qv_x = qE_z$  and  $E_z = B_y v_x = B_y I_x / btnq$

The Hall voltage is  $V_z = E_z b$   
 $V_z = B_y I_x / mqt = K_H B_y I_x / t$

$K_H$  is known as the Hall coefficient and should be as large as possible for maximum output. Conductivity is  $\sigma = qn\mu_n$  where  $\mu_n$  is electron mobility  $K_H = 1/qn = \mu_n / \sigma$

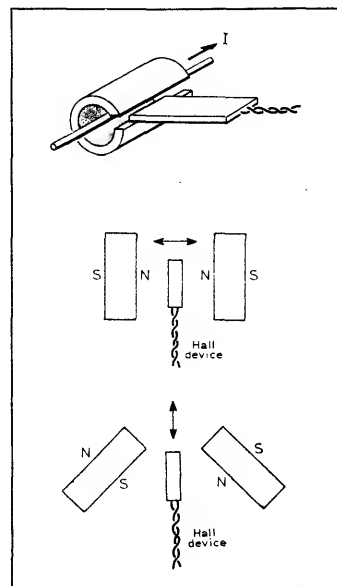
High mobility, low-conductivity optimizes device Hall voltage for specific thickness  $t$ .

**Applications**

- An appropriately dimensioned device can be inserted within the air gap flux-path of a rotating electrical machine to determine flux

density variations, when  $I_x$  is maintained constant.

- Both  $I_x$  and  $B_y$  can be generated by suitable voltages, and assuming fixed orientation between the Hall device and the field, then  $V_z \propto V_x V_y$ , where  $V_x$  and  $V_y$  may assume an alternating or direct voltage



identity.

Typical dimensions for insertion in thin gaps 0.006in and for axial probes 0.063in in diameter.

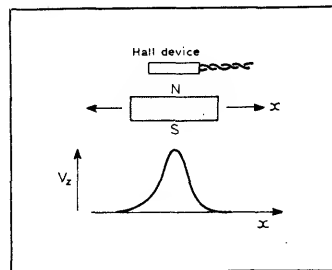
- A recent development<sup>1</sup>, is a Hall-effect magnetic field detector for translating information on the polarity and field strength of a magnetic field into a differential output current using integrated circuit technology (Mullard TCA450A). This device offers a high level of sensitivity, low offset flux and is self-balancing. Typical supply voltage 4-16V. Magnetic sensitivity 0.4V/Tesla.

Offset flux density  $\pm 7.5 \times 10^{-8}$  Tesla.

Possible applications include isolated current sensing and control in high current situations, conversion of magnetic quantities into proportional currents, detection of positional movements of a rotating shaft.

- **Current measurement.** Very small alternating and direct currents may be measured by concentrating the flux established around the conductor via the magnetic cylinder shown.

- **Linear displacement transducer.** The Hall device will produce a voltage which is a function of the motion



between the device and a stationary magnetic field. Displacement laterally between the magnets will produce an output voltage when the device is moved from the mid-position. An alternative arrangement will provide a linear output proportional to the displacement direction shown. In this case the magnetic field strength varies along a central plane.

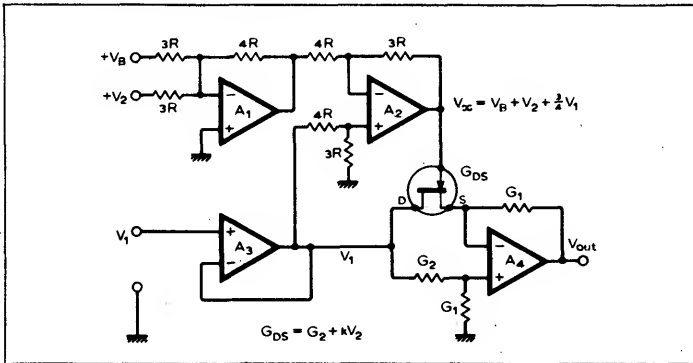
- **Proximity detector**  
A non-contact proximity

switch may detect the presence of a magnetic field or the disturbance of a field due to the presence of ferrous material. Hall voltage,  $V_z$ , variation in relation to relative position of magnetic and Hall device would be as shown.

**References**

- Chasmer, R. P., Cohen, E., Holmes, D. P. Design and performance of a Hall-effect multiplier, *Proc. IEE* 106 Part B. Supplement 16, 1959.
- Newsome, J. P. Application of the Hall effect. *Electronics & Power*, April 1966.
- 1. Mullard News Bulletin, 1975.

F.e.t. analogue multiplier



Circuit description

The conductance  $G_{DS}$  of the junction field-effect transistor depends on the voltage  $V_x$ . To linearize the f.e.t. in its pre-pinch-off region  $V_x$  must comprise one half of the sum of the separate drain and source voltages with respect to ground. In this case, that is equivalent to  $\frac{1}{2}(V_1 + V_1/2)$ . The total gate-voltage is then a fixed bias voltage  $V_B$ , a signal voltage  $V_2$  and the required  $\frac{3}{4}V_1$  is obtained via  $A_3$  and  $A_2$ . With then the equivalence of conductances  $G_1$ , the output voltage  $V_{out}$  is linearly proportional to the product of signals  $V_1$  and  $V_2$ , when  $G_{DS}$  is equal to  $G_2$  plus an incremental value proportional to  $V_2$ . Equating the potentials at the inverting and non-inverting inputs of amplifier  $A_4$  and using the parallel generator concept then

$$\frac{V_1(G_2 + KV_2) + V_{out}G_1}{G_1 + G_2 + kV_x} = \frac{V_1G_2}{G_1 + G_2}$$

This gives

$$V_{out} = -\frac{KV_1V_2}{G_1 + G_2}$$

The drain current drain-source voltage relationship is

$$I_D \propto (V_G - V_P - \frac{V_D + V_S}{2}) V_{DS}$$

If  $V_G$  does comprise  $V_B$ ,  $V_2$  and  $(V_D + V_S)/2$ , then  $G_{DS} = I_D/V_{DS} \propto (V_B - V_P + V_2)$  for pre-pinch-off.

If the constant of proportionality  $K_1 = K$ , and is such a value that  $K_1(V_B - V_P) = G_2$ , then a linearised relationship between the

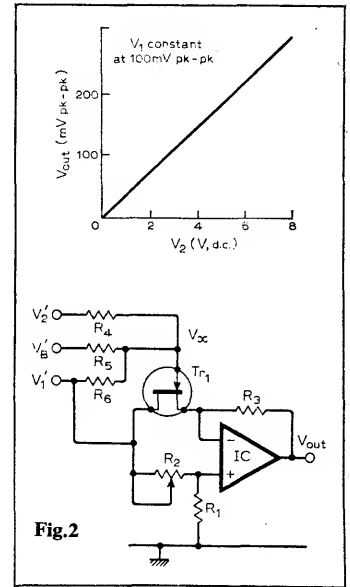
output and the product  $V_1V_2$  is achieved.

To demonstrate the principle, the circuit is simulated by Fig. 2, where if  $R_4 = R_5 = 6R$ ,  $R_6 = R$ , then  $V_x = \frac{3}{4}V_1 + V_2 + V_B'$ . To obtain the best linearity, these values of resistors need to be chosen empirically. This is most easily performed using an oscilloscope with an X-Y facility, where the input  $V_1$  and output for  $V_2$  zero volts are applied X-Y inputs respectively. Any non-linearity or offset can then be minimized by varying the resistors.

A more practical circuit (see reference) includes temperature compensation by making  $G_2$  another voltage dependent conductance, using a matched field-effect transistor (above). For maximum signal amplitudes, f.e.t.s with a high

Typical data (simulation)

IC SN741  $Tr_1$  2N5457  
 $R_1, R_3$  330 $\Omega$ ,  $R_2$  1k $\Omega$   
 $R_4, R_5$  22k $\Omega$ ,  $R_6$  6.8k $\Omega$   
 frequency 1KHz  
 $V_1$  maintained at 100mV pk-pk to achieve the best linearity. Linearity obtained is demonstrated on the graph.



pinch-off should provide a wider working range. Also if the gate bias  $V_B$  is arranged to be one half the pinch-off value, then

$$G_{DS} = K(-\frac{V_P}{2} + V_2)$$

i.e.  $G_2 = -\frac{KV_P}{2}$

and if  $G_1 = G_2$ , then

$$V_{out} = -V_1V_2K/2G_2 = \frac{V_1V_2}{V_P}$$

Typical pinch-off is  $-10V$  for results quoted, but no signal levels are identified.

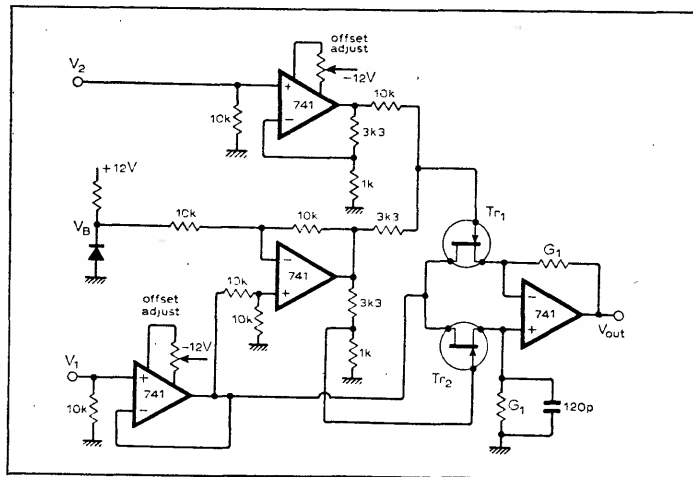
Accuracies claimed are within  $\pm 1\%$  over a temperature range of 50K in the frequency range 0 to 20kHz, using matched f.e.t.s whose conductances are within  $\pm 5\%$ .

Reference

Miller, A. Temperature compensated analogue multiplier, *Electronics Letters* 9 Sept. 1971, vol. 17, no. 18.

Related circuits

Set 22, card 7



Analogue circuit design is on the edge of another of its periodic revolutions. The development includes analogue multipliers of performance that permits function-synthesis to an accuracy that is limited mainly by the external passive components. One variant has three separate differential-input transconductance amplifiers: two drive a translinear multiplier core whose output is summed with that from the third to produce the final output via a high gain amplifier. The signals are processed throughout in current form but inputs and outputs are voltages

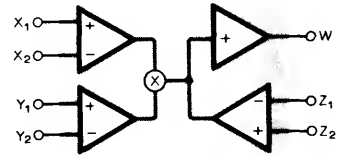
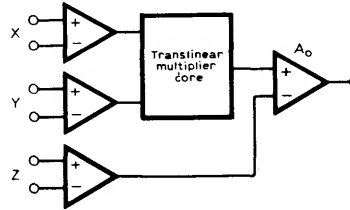
with the usual scaling factor so that  $W =$

$$\frac{10(X_1 - X_2)(Y_1 - Y_2) + Z_2 - Z_1}{10}$$

Normally overall feedback together with the large value of  $A_0$  ensures that the bracketed term tends to zero and the implicit identity

$$\frac{(X_1 - X_2)(Y_1 - Y_2)}{10} = Z_1 - Z_2$$

follows. The operation is analogous to that at the summing junction of an op-amp. A similar flexibility is obtained with higher order functions to that which we have become used to in linear



circuit design. To avoid the inconvenience of the scaling factor when devising new configurations it is helpful to write the variables in normalized from  $x, y, z:$

$$(x_1 - x_2)(y_1 - y_2) = z_1 - z_2.$$

To avoid confusion with the terminology of  $X$  and  $Y$  as multiplier inputs the more general input and output variables are written as  $U, V$  and  $W$  or  $u, v, w$  when normalized.

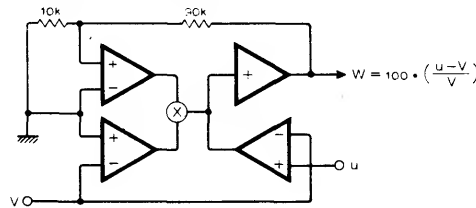
The reference article offers more than 20 applications many of them novel, and is essential reading for anyone who wants to exploit the possibilities of these new multipliers. At present they are precision devices laser-trimmed and are correspondingly priced but it is to be hoped that designers will overcome these limits and produce them at mass-market costs. A couple of examples indicate the simplicity of the solutions that are made possible by such circuits:

at the other extremes more complex configurations are claimed to yield trigonometric conversion functions with accuracies down to 0.01%.

The first circuit implements a percentage deviation computer

in which, for two input variables  $u$  and  $v$ , each of up to 10V, the output is one volt for each 1% difference between the variables

$$W = 100 \frac{U - V}{V}$$



This is established by observing

$$\begin{matrix} X_1 = W/10 & Y_1 = 0 & Z_1 = V \\ X_2 = 0 & Y_2 = V & Z_2 = U \end{matrix}$$

and substituting the second identity

$$\frac{(W/10)(-V)}{10} = V - U$$

$$W = 100 \frac{U - V}{V}$$

The feedback ratio can be adjusted to give 0.1V/% to 10V/% and the only restriction is that  $V$  must be positive.

An even simpler configuration has, in normalized form,

$$\begin{matrix} x_1 = w & y_1 = u & z_1 = w \\ x_2 = 0 & y_2 = 0 & z_2 = u \end{matrix}$$

Hence  $wu = w - u$  and

$$w = \frac{u}{1 - u}$$

This non-linearity is the exact inverse of that associated with a conventional Wheatstone bridge

viz  $u = v/(1 + v)$ . Hence a single multiplier can linearize the output of such transducers as strain-gauge bridges. The functions can be implemented by conventional multipliers but may need additional summing amplifiers and inverters, which in turn limit the accuracy and bandwidth claimed  $\pm 0.25\%$  and 1MHz with 35V/ $\mu$ s slew-rate.

### References

Gilbert, B. New analogue multiplier opens way to powerful function-synthesis, *Microelectronics*, 1976, vol.8, pp.26-36.

