A.4 Computing Circuits

Four versions of the inverting op amp and four versions of the noninverting op amp were given in the previous section. During the concept stage of the design, one of these eight op amp circuits is selected. Specifications for the input and output voltage are the selection criteria that determines which circuit configuration is used.

There are four versions of most of the circuits given in this and following sections, but just the simplest version of any circuit is included in this appendix because of space limitations. Each circuit configuration can be modified as required to fit specific applications. Look back to the first section to determine what bias is required to fit the application, and adapt that bias to the new circuit.

A.4.1 Inverting Summer

The three input voltages are inverted and added as Equation A–29 shows. R_B should be made equal in value to the parallel combination of R_F, R_{G1}, R_{G2}, and R_{G3} to convert the input bias current to a common-mode voltage so the op amp can reject it. V_{REF} sets the output voltage somewhere between the supply limits, and this allows negative addition (subtraction) to take place.

$$V_{OUT} = -\left(V_{IN1}\frac{R_F}{R_{G1}} + V_{IN2}\frac{R_F}{R_{G2}} + V_{IN3}\frac{R_F}{R_{G3}} + \ldots\right) + V_{REF}\left(1 + \frac{R_F}{R_{G1} \parallel R_{G2} \parallel R_{G3} \ldots}\right) \quad \text{A–29}$$

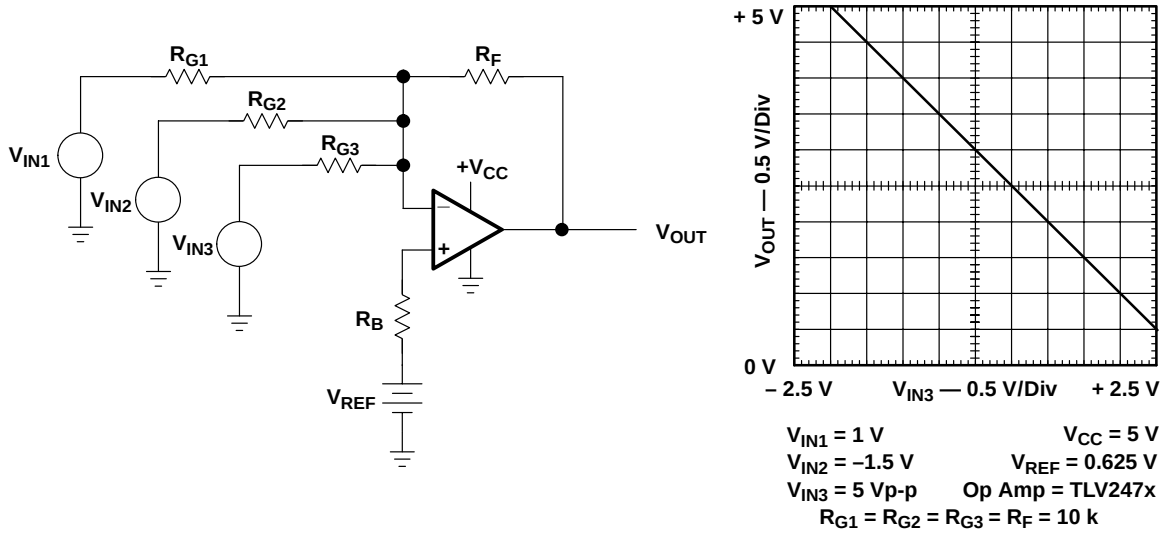

Figure A–24. Inverting Summer

A.4.2 Noninverting Summer

This circuit adds the input voltages and multiplies them by the stage gain. R_{G1}, R_{G2}, and R_{G3} in parallel should be equal to R_F in parallel with R_G to cancel the input bias current using the common-mode input voltage rejection technique. V_{REF} is added to the circuit to enable the addition of negative values.

$$V_{OUT} = + \left(\frac{V_{IN1}\left(R_{G2} \parallel R_{G3}\right)}{R_{G1} + R_{G2} \parallel R_{G3}} + \frac{V_{IN2}\left(R_{G1} \parallel R_{G3}\right)}{R_{G2} + R_{G1} \parallel R_{G3}} + \frac{V_{IN3}\left(R_{G2} \parallel R_{G1}\right)}{R_{G3} + R_{G2} \parallel R_{G1}} \right) \times \left(\frac{R_F + R_G}{R_G} \right) - V_{REF} \frac{R_F}{R_G} \qquad \text{A–30}$$

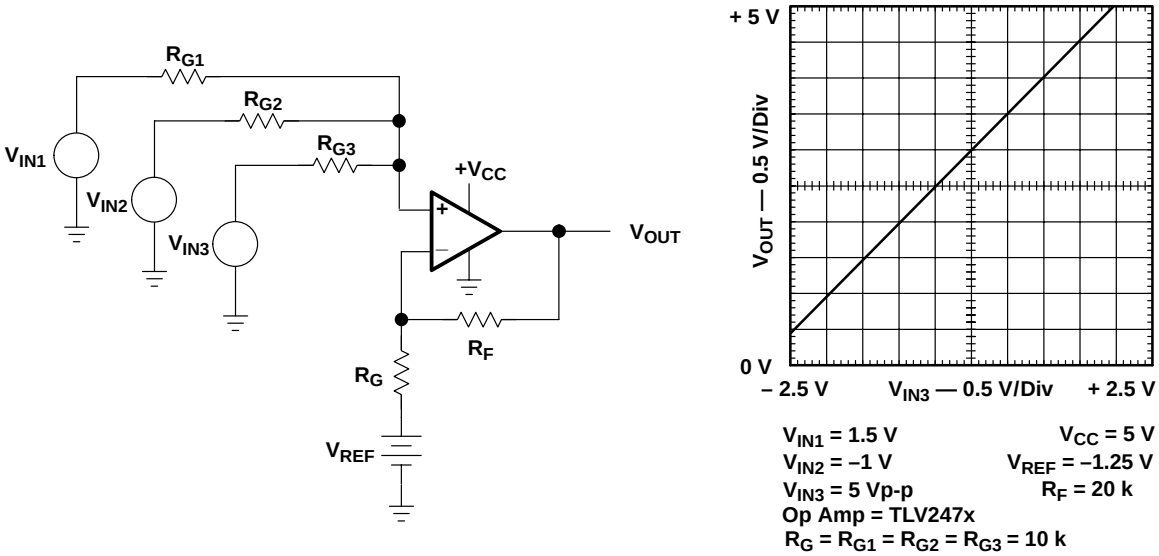

Figure A–25. Noninverting Summer

A.4.3 Noninverting Summer with Buffers

V_{REF1} and V_{REF2} are added to enable the buffers to handle positive input voltages. Their output contribution to the last stage is cancelled out by V_{REF3}. This configuration uses fewer resistors at the expense of two op amps. R_{G1}, R_{G2}, and R_F in parallel should be made equal to R_B to cancel the input bias current.

$$V_{OUT} = V_{IN1}\frac{R_F}{R_{G1}} + V_{IN2}\frac{R_F}{R_{G2}} - V_{REF1}\frac{2R_F}{R_{G1}} - V_{REF2}\frac{2R_F}{R_{G2}} + V_{REF3}\left(1 + \frac{R_F}{R_{G1} \parallel R_{G2}}\right) \quad \text{A–31}$$

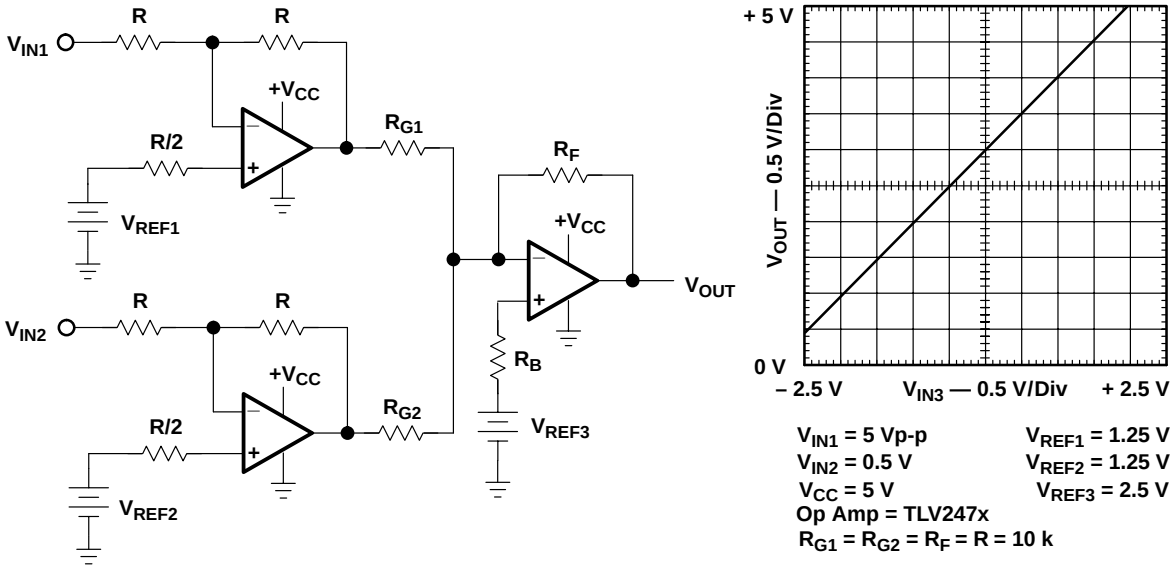

Figure A–26. Noninverting Summer with Buffers

A.4.4 Inverting Integrator

The Laplace operator, s= jω, is used in Equation A–32, and the mathematical operation 1/s constitutes an integration. Differentiation circuits are shown later, and the mathematical operation, s, constitutes a differentiation. The integration time constant is RC, thus the magnitude crosses 0 dB on a log plot when RC = 1. Also the phase is –45° when RC = 1.

$$V_{OUT} = - V_{IN} \frac{1}{RCs} \qquad \text{A–32}$$

This integrator is not very practical because there is no method of discharging the capacitor; hence, any leakage current will eventually charge the capacitor until the circuit becomes saturated. The positive input of the integrator is biased at V_{CC} / 2 to center the output voltage at V_{CC} / 2; thus allowing for positive and negative voltage swings. The bias resistors are selected as 2R so that the parallel combination equals R. This offsets the input current drawn through R.

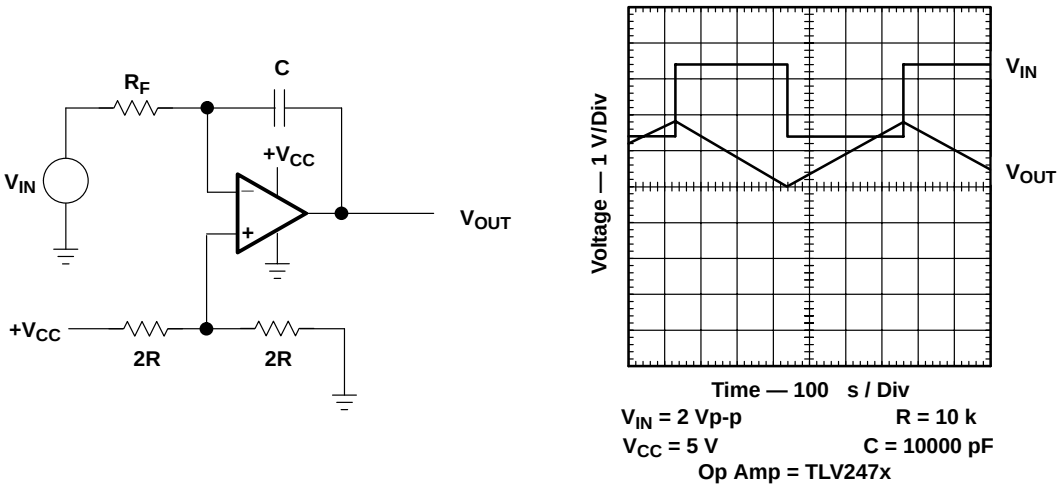

Figure A–27. Inverting Integrator

A.4.5 Inverting Integrator with Input Current Compensation

Functionally, this circuit is the same as that shown in Figure A–27, but a current compensation network has been added to offset the input current. V_{CC}, R_1, and R_2 bias the positive input at V_{CC} / 2 to center the output voltage at V_{CC} / 2; thus allowing for positive and negative voltage swings.

R_1 and R_2 are selected as relatively small values because the current flowing through R_A also flows through the parallel combination of R_1 and R_2. R_A forward biases the diode with a constant current, thus the diode acts like a small voltage regulator. The diode voltage drop is temperature sensitive, and this factor works in our favor because the input transistors are temperature sensitive. The two temperature sensitivities cancel out if the diode current is selected correctly. R_B is a large-value resistor that acts like a current source, so it is selected such that it supplies the input bias current. Selecting R_B correctly ensures that no input current flows through the integration resistor, R.

This integrator is not very practical because there is no method of discharging the capacitor. Hence, any input current will eventually charge the capacitor until the circuit becomes saturated. The bias circuit drastically reduces the input current flowing through R, thus it extends the integration time. A reset circuit is needed to make the integrator more practical.

This bias compensation scheme is set up for an op amp that has NPN input transistors. The diode must be reversed and connected to ground for op amps with PNP input circuits.

$$V_{OUT} = -V_{IN1}\frac{1}{RCs} \qquad \text{A–33}$$

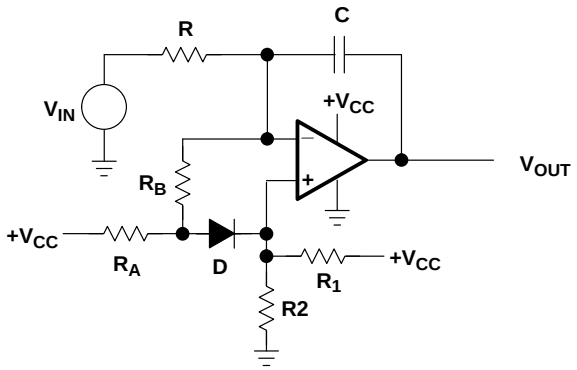

Figure A–28. Inverting Integrator with Input Current Compensation

A.4.6 Inverting Integrator with Drift Compensation

Functionally, this circuit is the same as that shown in Figure A–27, but it uses an RC circuit in the positive lead to obtain drift compensation. The voltage divider is made from a series string of resistors (R_A), and V_{CC} biases the input in the center of the power supply.

Positive input current flows through R and C in parallel, so the positive input current drops the same voltage across the parallel RC combination as the negative input current drops across its series RC combination. The common-mode rejection capability of the op amp rejects the voltages caused by the input currents. Much longer integration times can be achieved with this circuit, but when the input signal does not center around $V_{CC}/2$, the compensation is poor.

$$V_{OUT} = - V_{IN1} \frac{1}{RCs} \qquad \text{A–34}$$

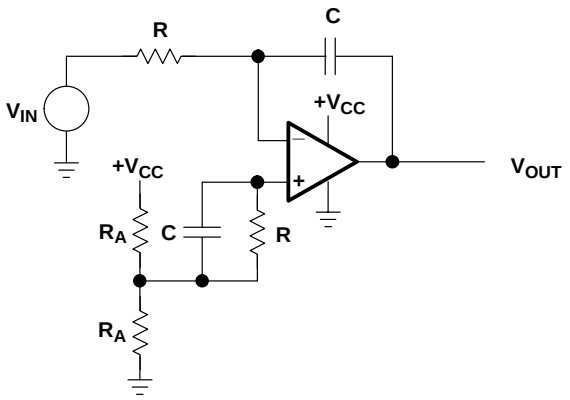

Figure A–29. Inverting Integrator with Drift Compensation

A.4.7 Inverting Integrator with Mechanical Reset

Functionally, this circuit is the same as that shown in Figure A–27, but a method has been provided to discharge (reset) the capacitor. S_1 is a mechanical switch or relay and when the contacts close, they short the integrating capacitor forcing it to discharge. Some capacitors are sensitive to fast discharge cycles, so R_S is put in the discharge path to limit the initial discharge current. When R_S is absent from the circuit, the impulse of current that occurs at the first instant of discharge causes considerable noise, so the selection of R_S is also based on noise considerations. For all practical purposes, the time constant formed by R_S and C determines the discharge rate.

One advantage of mechanical discharge methods is that they are isolated from the remainder of the circuit. Their size, weight, time delay, and uncertain actuating time offset this advantage. When the disadvantages of mechanical reset outweigh the advantages, circuit designers go to electronic reset circuits.

$$V_{OUT} = - V_{IN1} \frac{1}{RCs} \qquad \text{A–35}$$

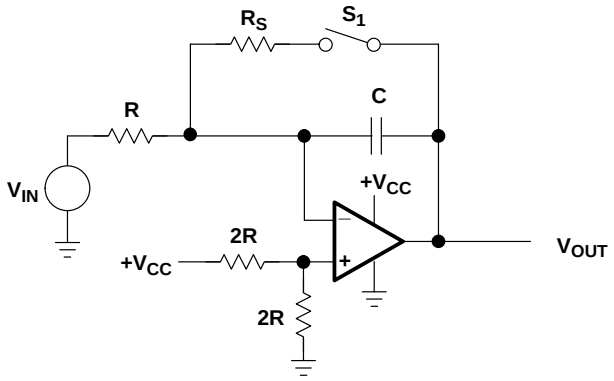

Figure A–30. Inverting Integrator with Mechanical Reset

A.4.8 Inverting Integrator with Electronic Reset

Functionally, this circuit is the same as that shown in Figure A–27, but an electronic method has been provided to discharge (reset) the capacitor. Q_1 is controlled by a gate drive signal that changes its state from on to off. When Q_1 is on, the gate-source resistance is low, less than 100 Ω. And when Q_1 is off, the gate-source resistance is high — about several hundred MΩ.

The source of the FET is at the inverting lead that is at ground, so the Q_1 gate-source bias is not affected by the input signal. Sometimes, the output signal can get large enough to cause leakage currents in Q_1, so the designer must take care to bias Q_1 correctly. Consult a transistor book for more detailed information on transistor reset circuits. A major problem with electronic reset is the charge injected through the transistor's stray capacitance. This charge can be large enough to cause integration errors.

$$V_{OUT} = -V_{IN1}\frac{1}{RCs} \qquad \text{A–36}$$

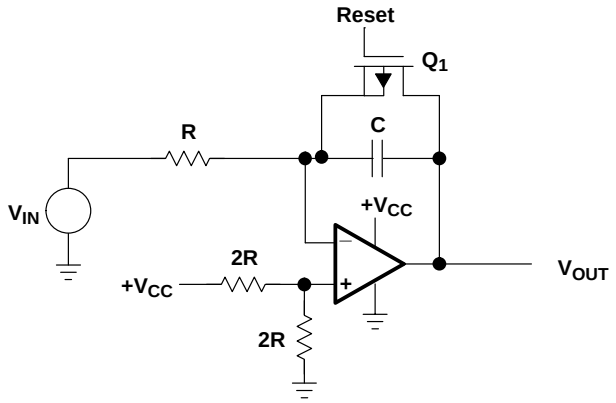

Figure A–31. Inverting Integrator with Electronic Reset

A.4.9 Inverting Integrator with Resistive Reset

This circuit differs from that shown in Figure A–27 because it yields a breakpoint rather than a pure integration. On a log plot, the integrator slope is –6 dB per octave at the 0 frequency intercept, and the 0 dB intercept occurs when f = 1/2πRC. A breakpoint plots flat on a log plot until the breakpoint where it breaks down at –6 dB per octave. It is –3 dB when f = 1/2πRC.

R_F is in parallel with the integrating capacitor, C, so it is continually discharging C. The low frequency attenuation that is the best attribute of the pure integrator is sacrificed for the reset circuit complexity

$$V_{OUT} = -V_{IN1}\left(\frac{R_F}{R_G}\right)\frac{1}{R_F C + 1} \qquad \text{A–37}$$

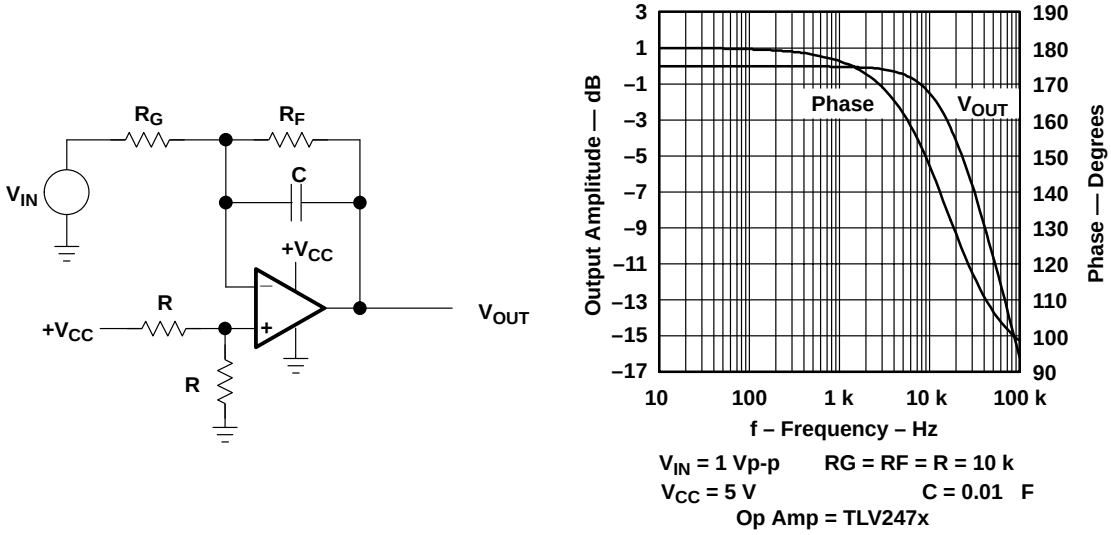

Figure A–32. Inverting Integrator with Resistive Reset

A.4.10 Noninverting Integrator with Inverting Buffer

This circuit is an inverting integrator preceded by an inverting buffer. Eliminating the signal inversion costs an op amp and four resistors, but this is the easiest way to get true noninverting integrator performance.

$$V_{OUT} = \frac{R_A}{R_A}\left(-V_{IN}\,\frac{1}{RCs}\right) = V_{IN}\,\frac{1}{RCs} \qquad \text{A–38}$$

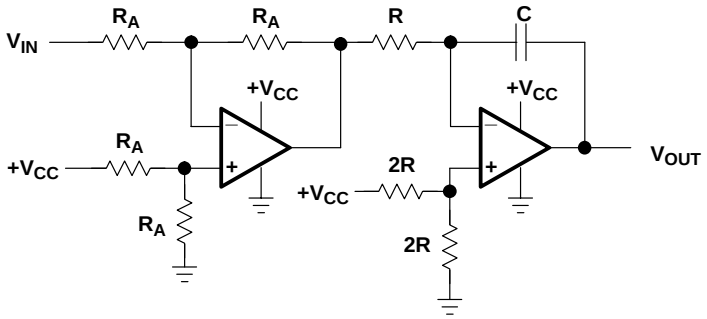

Figure A–33. Noninverting Integrator with Inverting Buffer

A.4.11 Noninverting Integrator Approximation

This circuit has fewer parts than the *Noninverting Integrator With Inverting Buffer* (Figure A–33), but it is not a true integrator because there is a zero in the transfer equation. The log plot starts rolling off at a –6 dB per octave rate at low frequencies, but when f = 1/2πRC, the zero cuts in. The zero causes the log plot to flatten out because the slope decreases to 0 db per decade.

This circuit functions as an integrator at very low frequencies, but at frequencies higher than f = 1/2πRC, it functions as a buffer.

$$V_{OUT} = \frac{RCs + 1}{RCs} \qquad \text{A–39}$$

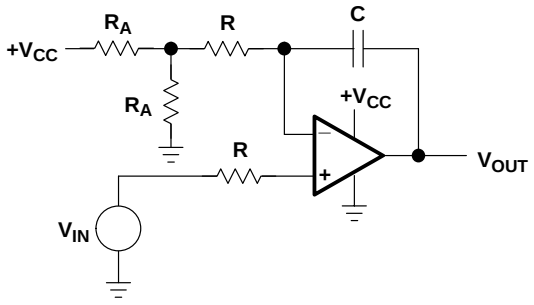

Figure A–34. Noninverting Integrator Approximation

A.4.12 Inverting Differentiator

The log plot of the differentiator is a positive slope of 6-dB per octave passing through 0 dB at f = 1/2πRC. At extremely high frequencies, the capacitive reactance goes to very low values, thus the circuit gain approaches the op amp open-loop gain. This performance emphasizes any system noise or noise generated by the op amp. The poor noise performance of this circuit limits its application to a very few specialized situations.

This configuration has a pole in the feedback loop. If the op amp has more than one pole, and most op amps have several poles, this configuration can become oscillatory. The V_{CC} and R_A circuit bias the output in the center of the power supplies. $R_A/2$ should be selected equal to $R_G||R_F$ so that input currents are canceled out.

$$V_{OUT} = - V_{IN} RCs \qquad \text{A–40}$$

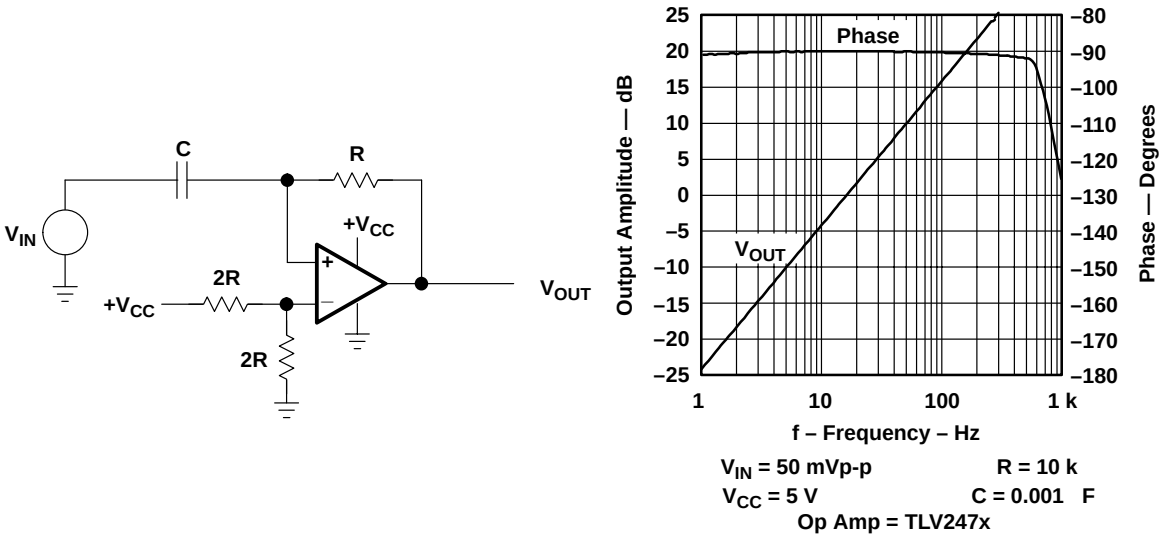

Figure A–35. Inverting Differentiator

A.4.13 Inverting Differentiator with Noise Filter

This circuit has a pure differentiator that rises at a 6-dB per octave slope from zero frequency. At $f = 1/2\pi R_F C_F$, the pole kicks in and the slope is reduced to zero. The pole has two effects. First, it stabilizes the circuit by canceling zero's phase shift. Second, it limits the circuit gain to 1 at high frequencies, so it acts like a noise filter.

R/2 should equal R_F for good input current cancellation, and V_{CC} coupled with R centers the output voltage.

$$V_{OUT} = - V_{IN} \frac{R_F C s}{R_F C_F s + 1} \qquad \text{A–41}$$

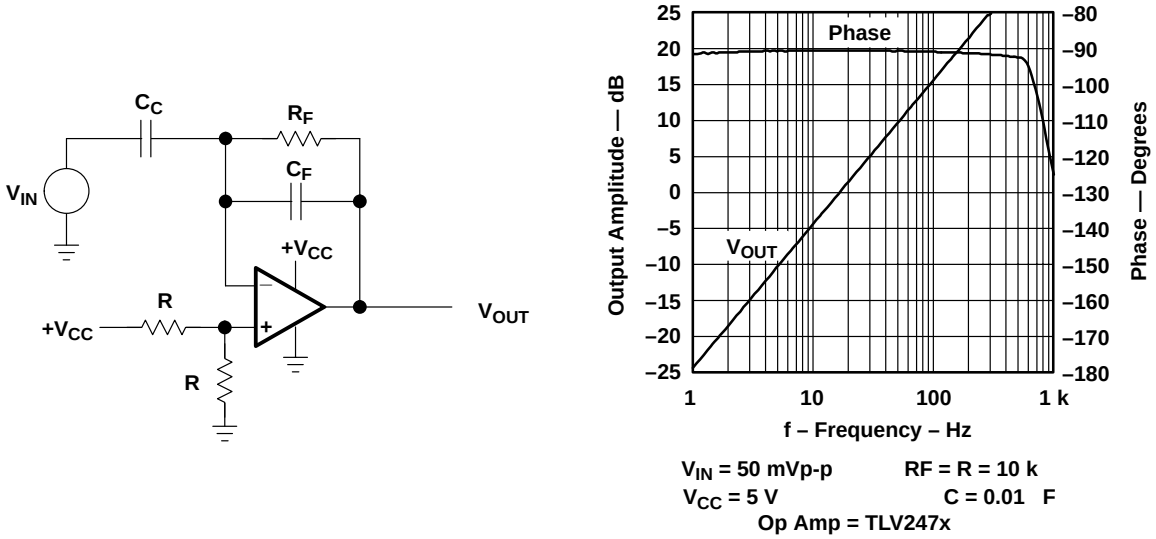

Figure A–36. Inverting Differentiator with Noise Filter