CHAPTER 2

25 A.C. AND D.C. AMPLIFIER PROJECTS

The high open-loop voltage gains and direct couplings of operational amplifiers enable the devices to be used in a wide variety of d.c. and a.c. amplifier applications. Because of the differential input facility of the op-amp, such amplifiers can be designed to be of either the inverting, the non-inverting, or the differential types.

When op-amps are used as closed-loop amplifiers the amplifier characteristics can, because of the high inherent gain of the op-amp, be dictated almost entirely by the values of external feedback components. By suitably selecting feedback networks, therefore, op-amps can readily be persuaded to act as precision linear amplifiers, as non-linear amplifiers, as frequency-selective amplifiers, or as constant-volume amplifiers, etc.

Twenty-five useful d.c. and a.c. amplifier projects of various types are shown in the present chapter. All of these circuits are designed around the popular type 741 integrated-circuit op-amp, and the pin connections shown in the following diagrams apply to the 8-pin dual-in-line version of this device only.

Inverting amplifier projects

An op-amp can be made to function as an inverting amplifier by grounding the positive input terminal and feeding the input signal to the negative terminal. If the amplifier is used in the open-loop mode the circuit will give a low-frequency voltage gain of about 100 000, and an input signal of a millivolt or so will be sufficient to drive the output to saturation. If the op-amp is used in the closed-loop mode, on the other hand, the circuit gain will be dictated by the values of the external feedback components, and almost any required values of voltage gain and input impedance can be obtained.

Figure 2.1a shows the connections for making an inverting d.c. amplifier with a voltage gain of 100, or 40 dB. Here, feedback resistor R_2 is wired between the op-amp output and the negative input terminal, and the input signal is applied to the negative input via R_1. The positive terminal is grounded via R_3.

There are two important facts to remember when looking at this circuit. First, the actual op-amp has a very high input impedance (typically 1 MΩ), so very little signal current flows into the negative input of the op-amp. The second point to remember is that the op-amp has a typical open-loop gain of 100 000 times. With these points in mind, consider the effect of R_2 on the circuit.

R_2 is wired as a negative feedback resistor between the output and the negative input terminal of the op-amp. Consequently, if an input of 100 μV is connected to the negative side of R_2, 10 volts will appear at the output and thus across R_2. The negative feedback thus effectively reduces the value of R_2 to R_2/A_{vo} where A_{vo} is the open-loop voltage gain of the op-amp. This modified resistance is effectively in parallel with the open loop input resistance of the op-amp, so the negative input appears as a 'virtual ground' low-impedance point.

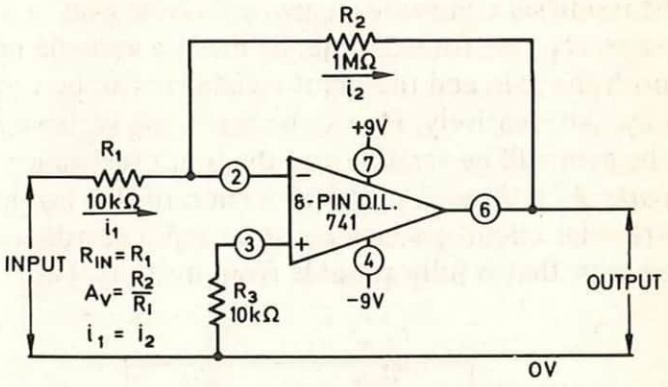


Figure 2.1a. x 100 inverting d.c. amplifier.

Although R_2 changes the input resistance of the amplifier, it has no effect on the voltage gain of the actual op-amp. The gain of the circuit (as opposed to the gain of the op-amp) is, however, changed by wiring R_1 in series between the circuits input terminal and the input of the op-amp. In this case R_1 and the 'virtual ground' resistance act effectively as a potential divider which causes only a fixed fraction of the input signal to be applied to the input of the op-amp, so reducing the gain of the overall circuit. The actual voltage gain, A_v, of the circuit works out at

$$A_v = \frac{R_2}{R_1 + \frac{R_2}{A_{vo}}}$$

In practice this formula simplifies to $A_v = R_2/R_1$ since A_{vo} is very large. The voltage gain of the *Figure 2.1a* circuit works out at $10^6/10^4 = 100$. Note that the voltage gain is dictated purely by the values of R_1 and R_2, and is virtually independent of variations in the op-amp characteristics.

There are three further points to note about this circuit. First, since the negative input terminal of the op-amp acts as a virtual ground, the input resistance of the circuit is equal to R_1. Hence, the basic circuit can be designed to give any required values of input resistance and voltage gain by choosing suitable values for R_1 and R_2.

The second point to note is that, since negligible current flows into the high-impedance negative terminal of the actual op-amp, any signal current that flows in R_1 must also flow in R_2, and signal currents i_1 and i_2 are thus equal.

Finally, note that the value of the R_3 resistor that is wired between the positive input and ground is chosen to give optimum thermal-drift performance of the op-amp, and should have a value equal to the parallel resistance of R_1 and R_2.

The *Figure 2.1a* circuit is designed to give a fixed voltage gain. The circuit can be modified and made to give a variable gain in a number of alternative ways. R_1 can, for example, be made a variable resistor, in which case both the gain and the input resistance can be varied simultaneously. Alternatively, R_2 can be made the variable resistor, in which case the gain will be variable and the input resistance will be constant. *Figure 2.1b* shows a practical version of this last-mentioned type, this particular circuit giving a constant input resistance of 10 kΩ amd a voltage gain that is fully variable from unity to 100.

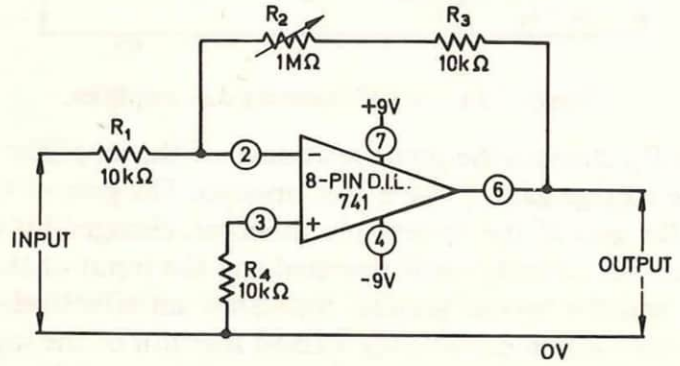


Figure 2.1b. Variable gain (x 1 to x 100) inverting d.c. amplifier.

A variation of the fixed-gain inverting d.c. amplifier is shown in *Figure 2.2a*. In this case potential divider $R_3 - R_4$ is wired across the op-amp output, and negative feedback resistor R_2 is wired between the $R_3 - R_4$ junction and the negative input terminal. This configuration

enables both R_1 and R_2 to be given high values while still giving high voltage gain. The voltage gain is given by

$$A_v = \frac{R_2}{R_1} \times \frac{R_3 + R_4}{R_4}$$

The *Figure 2.2a* circuit has an input resistance of 1 MΩ, and a voltage gain of 100.

The *Figure 2.2a* circuit can be made to give a variable gain in any one of a number of ways. The gain can be made variable by changing the value of any one of the four resistors, or by replacing $R_1 - R_2$ or

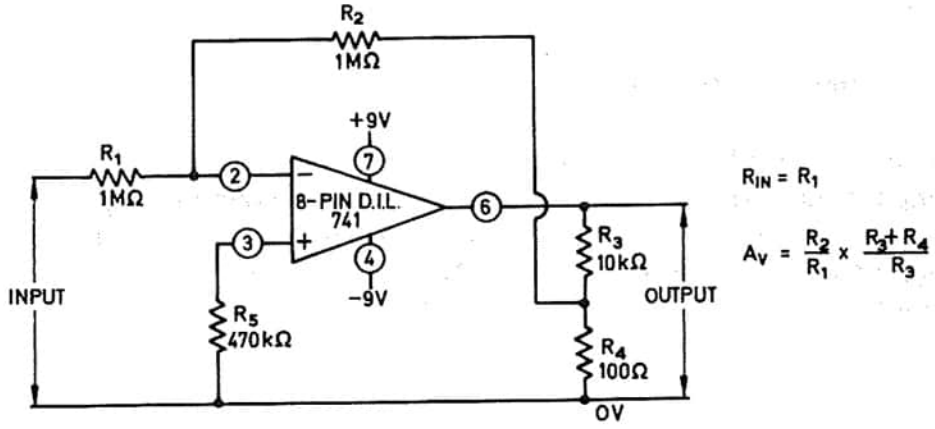


Figure 2.2a. High-impedance x 100 inverting d.c. amplifier.

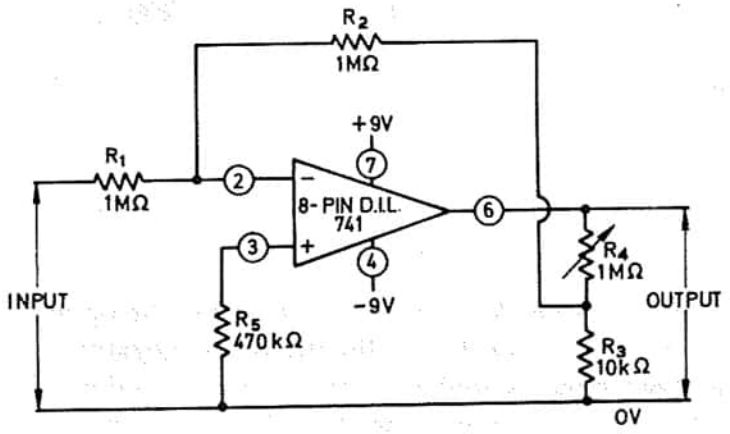


Figure 2.2b. High-impedance, variable gain (x 1 to x 100) inverting d.c. amplifier.

$R_3 - R_4$ by a variable potential divider. *Figure 2.2b* shows how the gain can be varied via R_4, while retaining a constant input resistance of 1MΩ to the amplifier.

The inverting circuits shown so far are used as d.c. amplifiers. They can readily be modified for a.c. use by simply wiring blocking capacitors in series with their inputs and outputs, as shown in the fixed gain inverting a.c. amplifier of *Figure 2.3.*

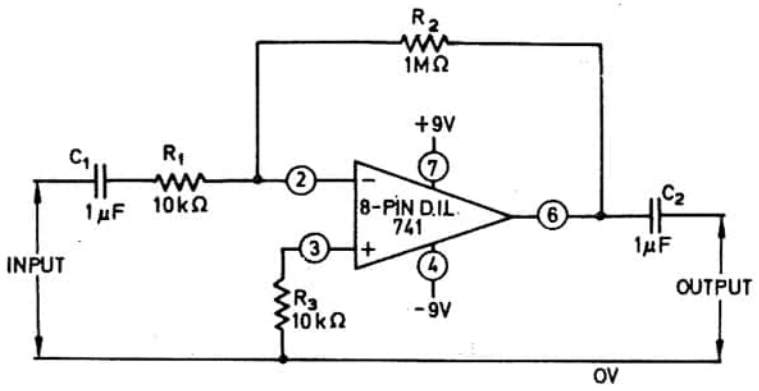


Figure 2.3. x 100 inverting a.c. amplifier.

Non-inverting amplifier projects

An op-amp can be made to function as a non-inverting amplifier by feeding the input signal to the positive terminal and applying negative feedback to the negative terminal via a resistive potential divider that is connected across the op-amp output. *Figure 2.4a* shows the connections for making a fixed gain (x 100) d.c. amplifier.

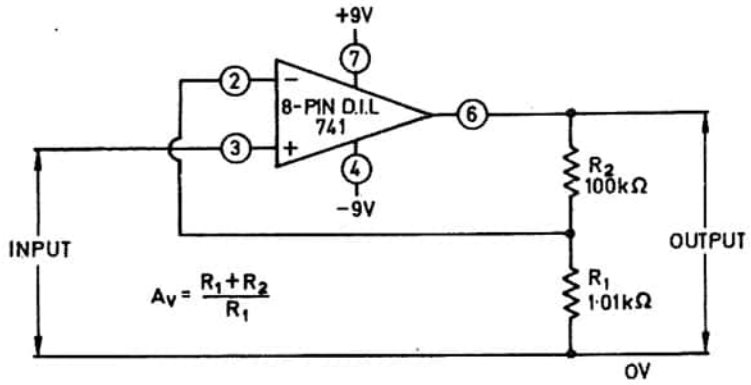


Figure 2.4a. Non-inverting x 100 d.c. amplifier.

Here, potential divider $R_1 - R_2$ is wired across the op-amp output, and the $R_1 - R_2$ junction is taken directly to the negative input of the op-amp; the input signal is applied to the positive terminal. The output signal is in phase with the input, and the voltage gain, A_v, is related to the values of R_1 and R_2 by the formula

$$A_v = \frac{R_1 + R_2}{R_1}$$

Hence, if R_2 is given a value of zero the gain falls to unity, and if R_1 is given a value of zero the gain rises towards infinity (but in practice is limited to the open-loop gain of the op-amp). The gain of the *Figure 2.4a* circuit works out at 100.

A major advantage of the non-inverting d.c. amplifier is that it gives a very high input impedance to the positive terminal. In theory the input resistance is equal to the open-loop input resistance (typically 1 MΩ) multiplied by the open-loop voltage gain (typically 100 000) divided by the actual circuit voltage gain. In practice input resistance values of hundreds of megohms can readily be obtained.

The basic fixed-gain non-inverting d.c. amplifier circuit of *Figure 2.4a* can be made to give a variable gain by replacing either R_1 or R_2 with a variable resistor, or by replacing R_1 and R_2 with a variable potential divider. *Figure 2.4b* shows the practical circuit of a variable gain d.c. amplifier, in which the gain can be varied from unity to 100 via a variable resistor in the R_2 position.

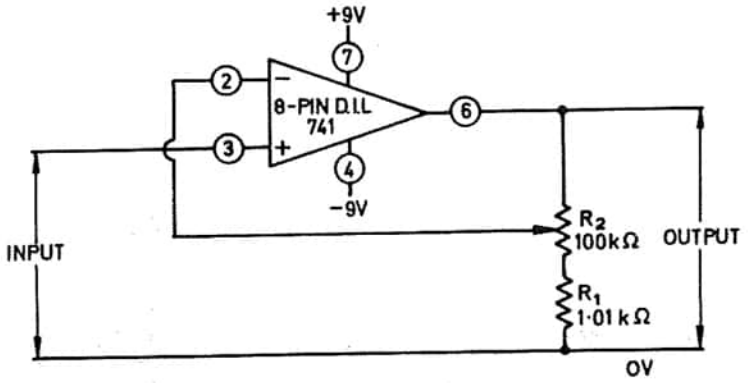


Figure 2.4b. Non-inverting variable gain (x 1 to x 100) d.c. amplifier.

The basic non-inverting d.c. circuits of *Figure 2.4a* and *2.4b* can be modified to operate as a.c. amplifiers in a variety of ways. The most obvious approach here is to simply wire blocking capacitors in series with the inputs and outputs, but in such cases the positive input must be d.c. grounded via a suitable resistor, as shown by R_3 in the fixed-gain non-inverting a.c. amplifier of *Figure 2.5*. If this resistor is not used the op-amp will have no d.c. stability, and its output will rapidly drift into

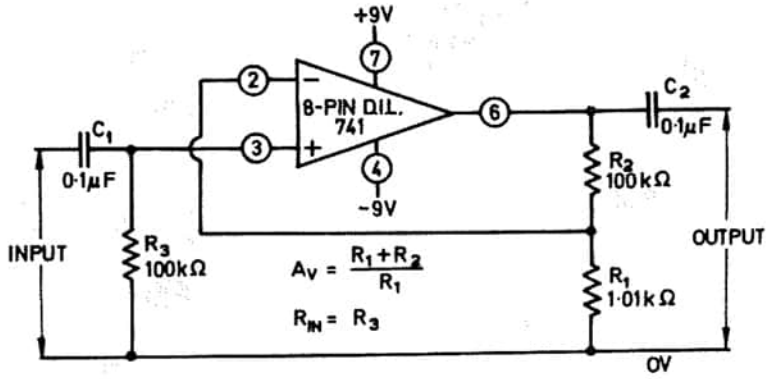


Figure 2.5. Non-inverting x 100 a.c. amplifier.

saturation. Clearly, the input resistance of the *Figure 2.5* circuit is equal to R_3 at operating frequencies, and R_3 must have a relatively low value in the interest of d.c. stability. This circuit thus loses the non-inverting amplifiers basic advantage of high input resistance. The *Figure 2.5* circuit has an input resistance of only 100 kΩ.

A useful development of the *Figure 2.5* circuit is shown in *Figure 2.6*. Here, blocking capacitor C_3 is wired in series with gain-determining potential-divider $R_1 - R_2$, and the $R_2 - C_3$ junction is taken directly to the negative input. The circuit thus has virtually 100 % d.c. negative feedback, gives near-unity d.c. voltage gain, and has excellent d.c. stability. As far as a.c. is concerned, however, C_3 acts as a short circuit, so the circuit gives an a.c. voltage gain of $(R_1 + R_2)/R_1$. Thus, the circuit has a closely controlled a.c. gain, with excellent d.c. stability. The input impedance is equal to R_3, and has a value of 100 kΩ.

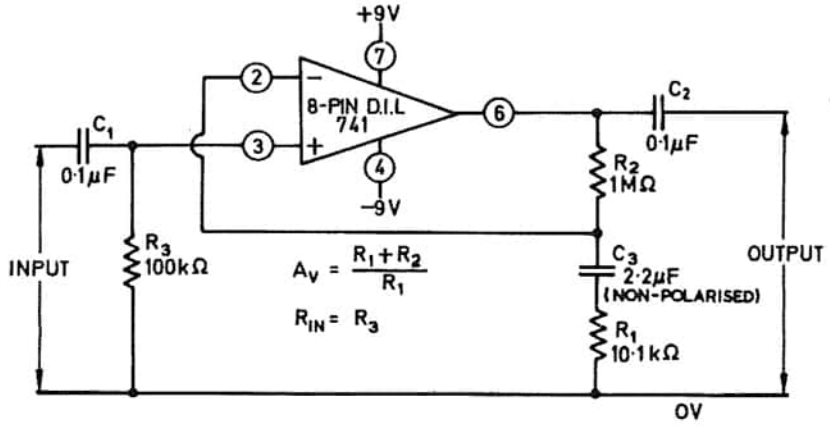


Figure 2.6. Non-inverting x 100 a.c. amplifier with d.c. negative feedback.

The *Figure 2.6* circuit can be further modified, so that it gives a very high input impedance, by using the connections shown in *Figure 2.7*. Here, the low end of input resistor R_3 is taken to the $C_3 - R_1$ junction,

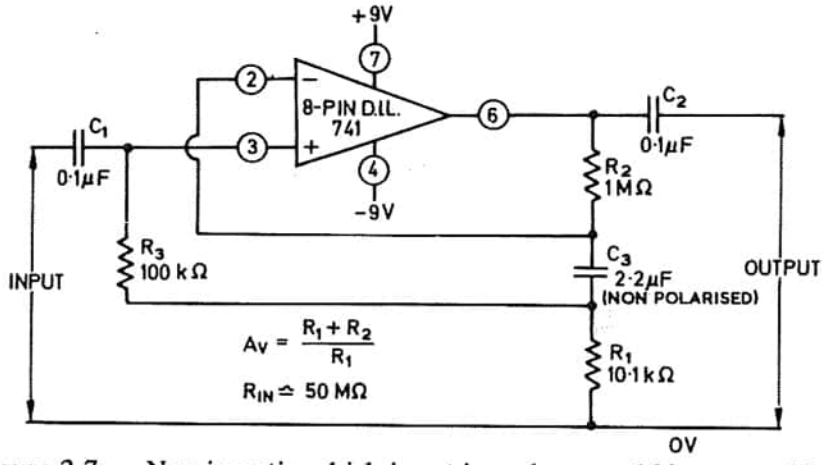


Figure 2.7. Non-inverting, high input-impedance, x 100 a.c. amplifier.

rather than directly to ground. Under a.c. amplifying conditions identical a.c. signals appear at the positive terminal of the op-amp and at the $R_1 - C_3$ junction of the gain-determining potential divider. Identical a.c. signals thus appear at each end of input resistor R_3, so zero signal current flows in this resistor, which consequently appears as a near-infinite resistance to a.c. signals. As a result, the circuit has a very high input resistance (typically of the order of 50 MΩ) as far as a.c. is concerned, but has good d.c. stability due to the fact that a relatively low d.c. resistance path exists between the positive terminal and ground (110 kΩ in this case), and that the circuit has near-unity d.c. gain due to the virtually 100 % d.c. negative feedback that is obtained via R_2.

The use of offset null

The op-amp is a direct-coupled device, and amplifies any d.c. or a.c. signal that appears at its input terminals. Ideally, when the op-amp is used in the open-loop mode, its output should register zero volts when its input terminals are grounded. In practice, however, the output usually goes to saturation under this condition, because internally generated voltages effectively apply a small offset or bias potential to the input circuitry of the op-amp. Typically, this 'differential input offset voltage' has a value of one or two millivolts, and this small d.c. voltage is amplified by the open-loop gain of the op-amp, and drives the output to saturation.

When the op-amp is used in the closed loop mode, the input offset voltage is amplified by a factor equal to the closed loop gain of the circuit. If the op-amp is used as a x 100 d.c. amplifier, and has an input offset potential of 2 mV, an output offset of 200 mV will be obtained when zero volts are applied to the input terminals.

In many applications this offset of the output is undesirable, so most op-amps have some facility for externally nulling or cancelling the effects of the offset voltage. In the case of the 8-pin dual-in-line version of the 741 op-amp, offset nulling is achieved by wiring a 10 kΩ variable potential divider, or pot, between null pins 1 and 5 of the op-amp, and taking the pot slider to the negative supply rail of the circuit. *Figure 2.8* shows the practical connections for applying the offset null facility to a x 100 non-inverting d.c. amplifier. The facility can be applied to any circuit that uses a 741 op-amp, but alternative pin connections may have to be used if types other than the 8-pin d.i.l.* version are used.

Voltage follower circuits

An op-amp can be made to function as a precision voltage follower by connecting it as a unity-gain non-inverting amplifier. *Figure 2.9a* shows

*d.i.l. or DIP

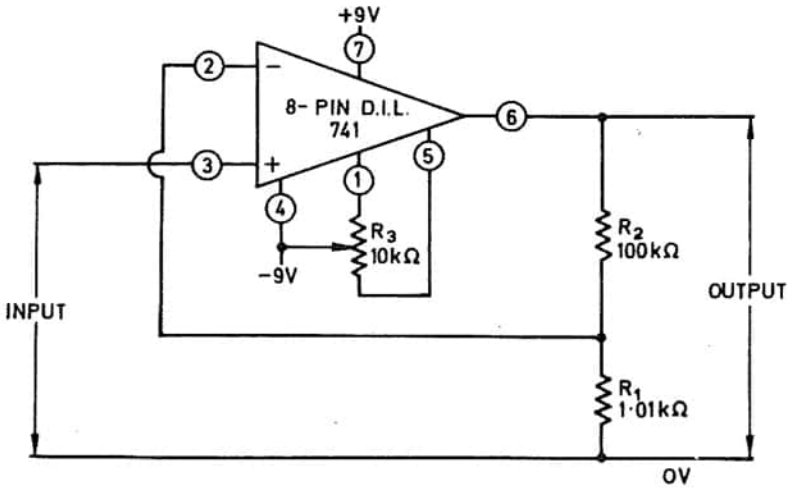


Figure 2.8. Non-inverting x 100 d.c. amplifier with offset null.

the practical connections for making a precision d.c. voltage follower. Here, the input signal is applied directly to the positive terminal of the op-amp, and the negative terminal is connected directly to the output, so the circuit has 100 % d.c. negative feedback and acts as a unity-gain non-inverting d.c. amplifier. The output voltage signal of the circuit is virtually identical to that at the input, so the output is said to 'follow' the input voltage. The great advantage of the circuit is that it has a very high input impedance (as high as hundreds of megohms) and a very low output impedance (as low as a few ohms). The circuit effectively acts as an impedance transformer.

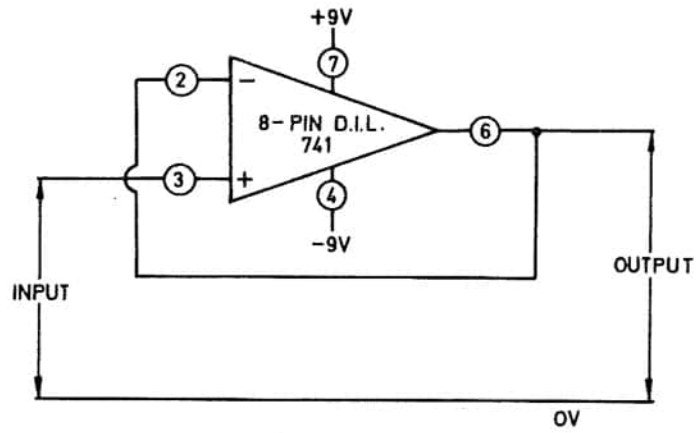


Figure 2.9a. D.C. voltage follower.

In practice the output of the basic *Figure 2.9a* circuit will follow the input to within a couple of millivolts up to magnitudes within a volt or so of the supply line potentials. If required, the circuit can be made to follow to within a few microvolts by adding the offset null facility to the op-amp.

Figure 2.9b shows how the *Figure 2.9a* circuit can be modified so that it acts as an a.c. voltage follower. Here, C_1 is wired in series with the input to block d.c. from the positive terminal, and C_2 is used to block d.c. from the output. R_1 is wired between the positive terminal and ground to provide a discharge path for C_1 and to ensure d.c. stability of the op-amp. Because of the presence of this resistor, the circuit has a resistive input impedance of only 1 MΩ.

Figure 2.9c shows how the a.c. voltage follower circuit can be modified so that it gives a resistive input impedance of hundreds or thousands of megohms. Here, the low end of input resistor R_1 is taken to ground via R_2, and the $R_1 - R_2$ junction is a.c. coupled to the op-amp

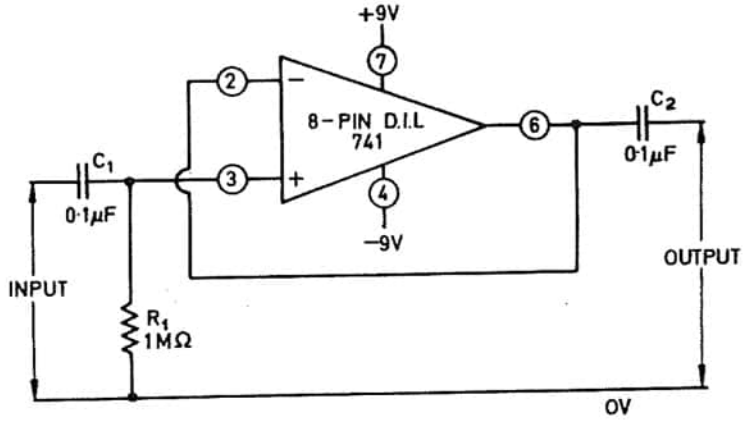


Figure 2.9b. A.C. voltage follower.

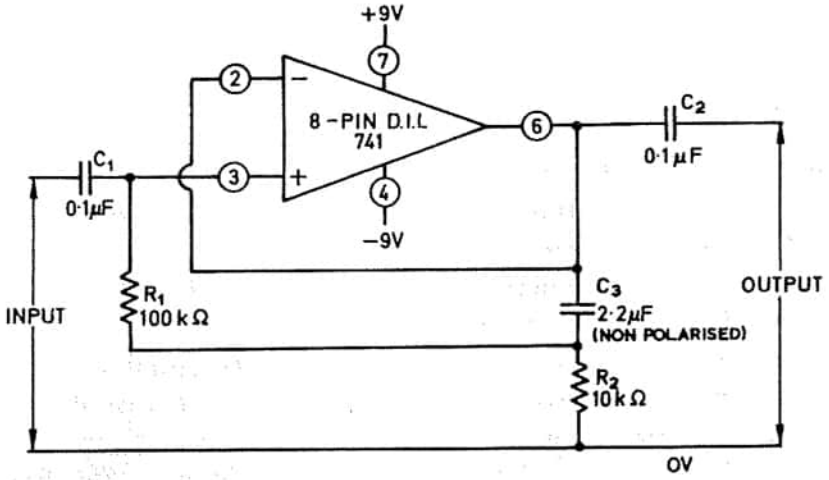


Figure 2.9c. Very high input-impedance a.c. voltage follower.

output via C_3. At a.c. operating frequencies C_3 appears as a virtual short circuit, so the full output signal of the op-amp appears at the $R_1 - R_2$ junction. Since the input and output signals of the circuit are identical, therefore, identical a.c. signals appear at both ends of R_1, and zero signal

current flows in this resistor, which thus appears as a near-infinite impedance to a.c. This technique of increasing the apparent value of a resistor is known as *bootstrapping*, and the technique enables the *Figure 2.9c* circuit to exhibit an input impedance of hundreds or thousands of megohms.

The 741 op-amp is capable of providing output currents up to about 5 mA, and this is consequently the current-driving limit of the three voltage follower circuits that we have looked at so far. If required, however, the current-driving capabilities of the circuits can readily be increased by wiring one or more emitter follower buffer stages between the op-amp output terminals and the output of the actual circuit. The precise design of the buffer stage depends on the output requirements of the circuit.

Figure 2.10a shows the practical circuit of an unidirectional d.c. voltage follower with a boosted output. Transistor Q_1 is an npn type,

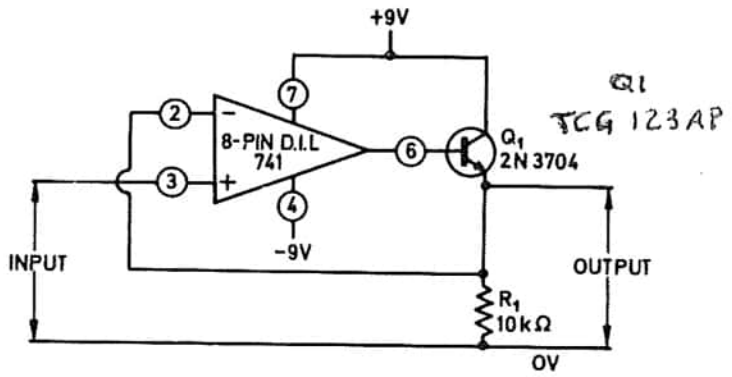


Figure 2.10a. Unidirectional d.c. voltage follower with boosted output (variable from 0 V to +8 V at 50 mA).

and is wired as an emitter follower between the op-amp output terminal and the output of the actual amplifier. Note that the negative feedback loop to the negative terminal of the op-amp is taken from the emitter of Q_1, so the base-emitter junction of the transistor is included in the negative feedback loop. Consequently, the effective value of the 600 mV base-emitter volt drop of Q_1 is reduced by a factor equal to the open-loop gain of the op-amp, so Q_1 has no significant effect on the voltage-following capabilities of the circuit. Q_1 does, however, boost the current-driving capability of the circuit to about 50 mA. This figure of 50 mA is dictated by the limited power rating of the 2N3704 transistor. Greater output currents can be obtained by replacing Q_1 with a high-gain power transistor.

Note that this particular circuit is capable of giving a positive output only, since Q_1 is an npn transistor and must be positively biased to operate. The circuit thus acts as an unidirectional voltage follower.

Figure 2.10b shows the practical circuit of a bidirectional d.c. voltage follower with boosted output. This circuit can provide both positive and negative outputs, with currents up to 50 mA mean or about 350 mA peak. Circuit operation is quite simple. $Q_1 - Q_2$ are wired together as a complementary emitter follower so that when the output is positive Q_1 is biased on and provides the output current, and Q_2 is cut off; or when the output is negative, Q_2 is biased on and provides the output current, and Q_1 is cut off: bidirectional outputs are thus available. Note that the base emitter junctions of both transistors are included in the negative feedback loop of the circuit, so these junctions consequently have negligible effect on the voltage following capabilities of the circuit. Slight loss of voltage following capability does, however, occur at near-zero output voltage levels, and may manifest itself in the form of cross-over distortion when the circuit is driven from an a.c. source.

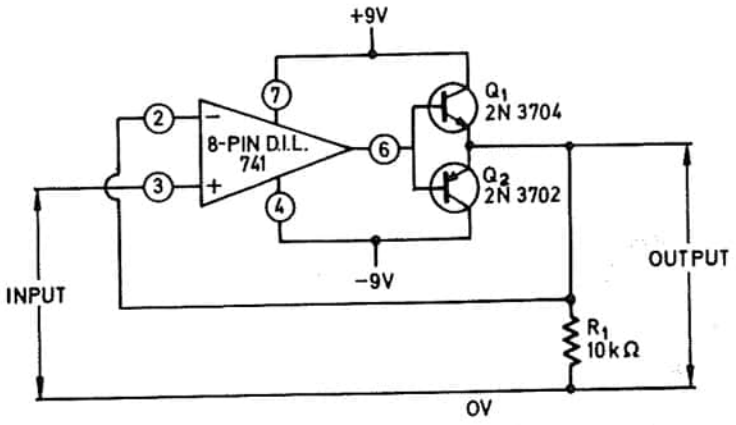


Figure 2.10b. Bidirectional d.c. voltage follower with boosted output (variable from 0 V to ±8 V at 50 mA).

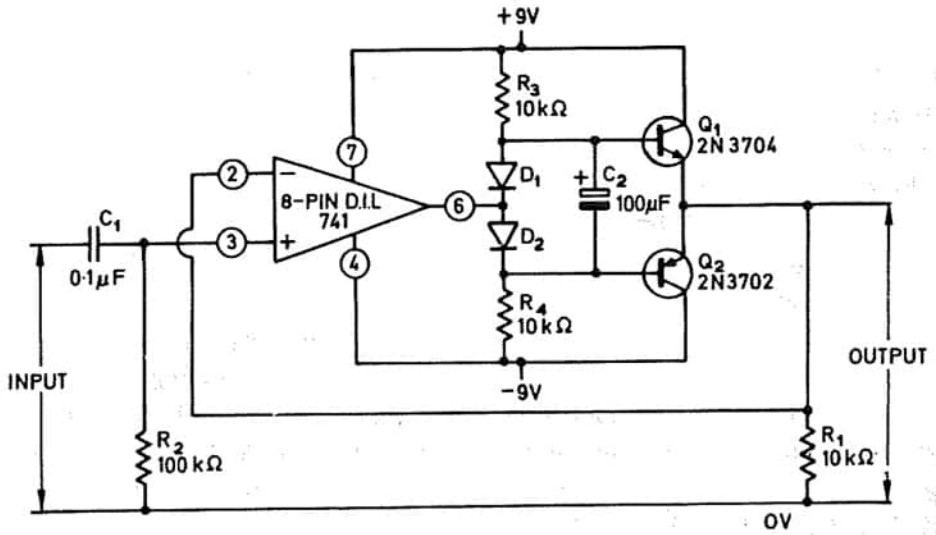


Figure 2.10c. Improved bidirectional follower with boosted output and a.c. input.

The improved bidirectional voltage follower circuit of *Figure 2.10c* shows how cross-over distortion can be reduced to negligible proportions by applying a small standing bias to each output transistor via potential divider $R_3 - D_1 - D_2 - R_4$. D_1 and D_2 are general-purpose silicon diodes. The circuit shows the connections to be used with an a.c. input, and C_2 is used to equalise the base drives to Q_1 and Q_2 at normal operating frequencies and so minimise distortion.

Addition circuits

An operational amplifier can be made to carry out the function of addition by connecting it as a multi-input inverting amplifier, as shown in the unity-gain inverting d.c. adder circuit of *Figure 2.11*. Looking at each input network individually, it can be seen that each input resistor combines with negative feedback resistor R_4 to form a unity-gain

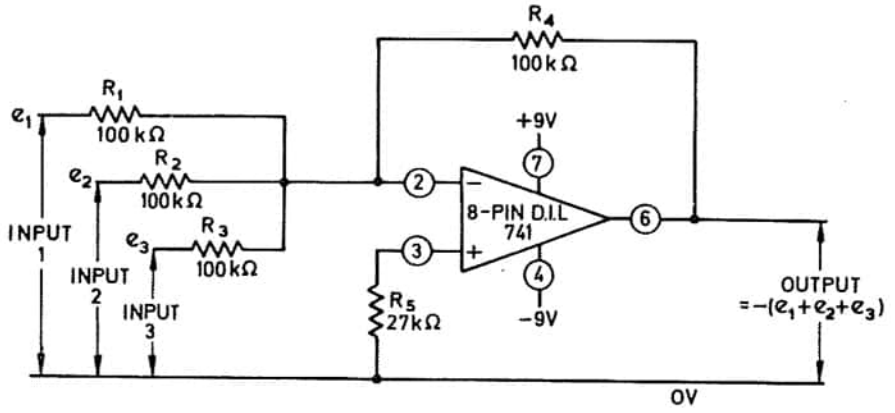


Figure 2.11. Unity-gain inverting d.c. adder.

inverting d.c. amplifier. A feature of the inverting amplifier is that virtually all of the input signal current flows through the negative feedback resistor, so the current flow in R_4 in the *Figure 2.11* circuit is equal to the sum of the three input signal currents of R_1, R_2, and R_3. Since resistors R_1 to R_4 all have equal values, therefore, the circuit gives an output voltage that is equal to the sum of the three input voltages, but is inverted in sign or polarity.

The *Figure 2.11* circuit can be made to give an output that is equal to the sum of any required number of inputs by simply wiring extra input resistors to the circuit. If required, the circuit can be made to give addition with gain by either increasing the value of R_4 or by reducing the values of all of the input resistors: the formula for the voltage gain is $A_v = R_4/R_{in}$, where R_{in} is the input resistor.

The *Figure 2.11* inverting adder circuit can be adapted for a.c. use by wiring blocking capacitors in series with each input resistor and with the

output. Adding circuits of this type are widely used as so-called 'mixers' in audio applications, the signal to each input terminal being made adjustable via a variable potential divider.

The *Figure 2.11* circuit gives an output that is inverted in sign relative to the input signals. The circuit can be made to give a non-inverted output that is truly equal to the sum of the input voltages by simply wiring an additional unity-gain inverting amplifier between the output of the adder stage and the output of the complete circuit, as shown in the non-inverting unity-gain d.c. adder circuit of *Figure 2.12.*

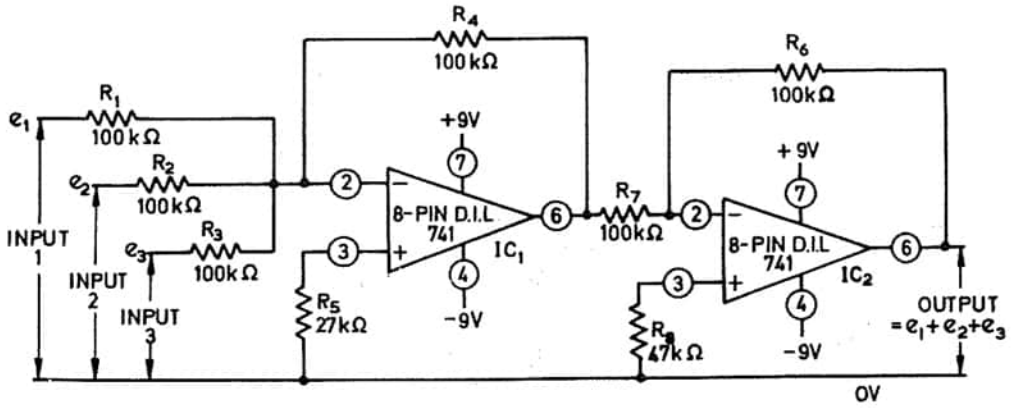


Figure 2.12. Non-inverting unity-gain d.c. adder.

Phase splitter circuits

Pairs of op-amps can be used to make precision balanced phase splitters by wiring the individual op-amps as unity-gain inverting amplifiers, and connecting the two amplifiers in series, as shown in *Figure 2.13*. Here, the output of IC_1 is connected directly to the input of the IC_2 amplifier stage. Consequently, the output of IC_1 is equal in

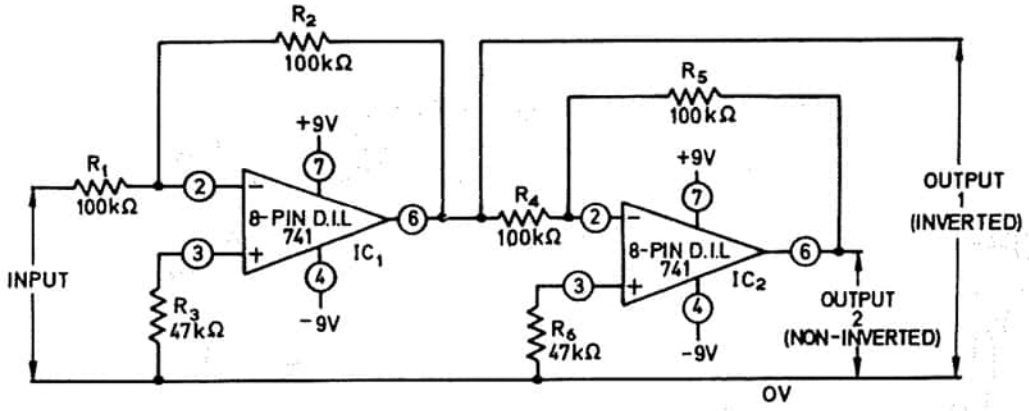


Figure 2.13. Unity-gain balanced d.c. phase-splitter.

amplitude but opposite in phase or polarity to the input signal, and the output of IC_2 is equal in amplitude but opposite in phase to the output of IC_1, and is thus in phase with the input. The two outputs are thus equal in amplitude but opposite in phase relative to each other, and the circuit acts as a unity-gain balanced d.c. phase splitter.

The circuit can be made to give balanced phase-splitting with gain, if required, by simply increasing the gain of the IC_1 inverting amplifier stage. *Figure 2.14* shows the connections for making a variable-gain balanced d.c. phase-splitter. The gain of this circuit can be varied between unity and x 100 via R_3.

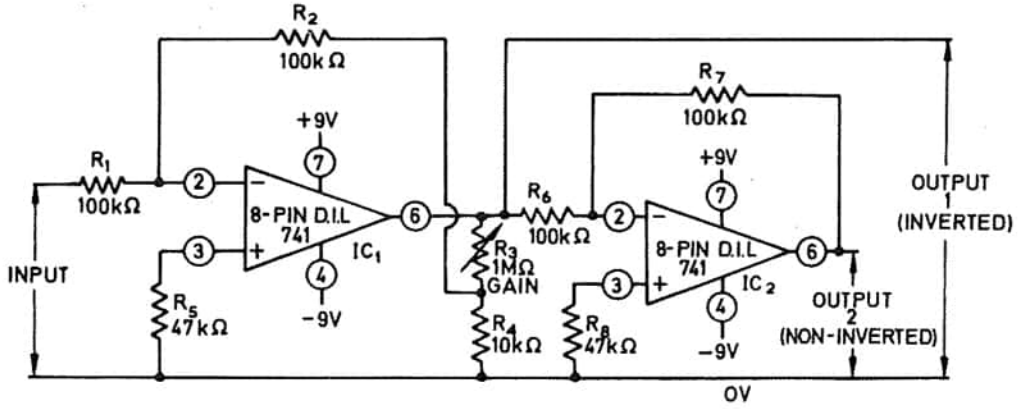


Figure 2.14. Variable-gain (x 1 to x 100) balanced d.c. phase-splitter.

The *Figure 2.13* and *2.14* circuits each have an input resistance of 100 kΩ. In some applications a far greater input resistance than this may be required. In such cases the very-high-impedance variable-gain balanced d.c. phase splitter of *Figure 2.15* can be used. This circuit has an input impedance of hundreds of megohms, and its gain is variable from unity

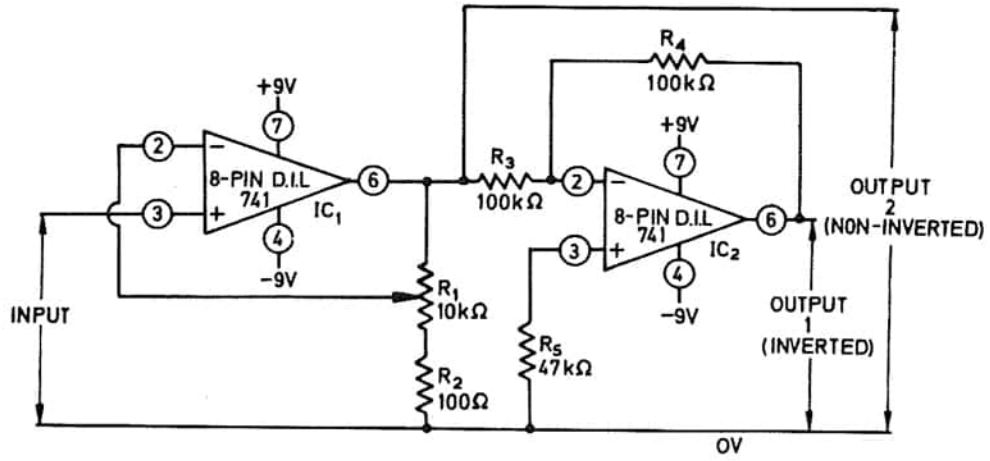


Figure 2.15. Very-high-impedance variable-gain (x 1 to x 100) balanced d.c. phase-splitter.

to x 100 via R_1. IC_1 in this circuit is wired as a variable-gain non-inverting amplifier, with its output feeding directly into the input of the unity-gain inverting stage that is wired around IC_2. The output of IC_1 is in phase with the input signal, and the output of IC_2 is in anti-phase.

Differential amplifiers or subtractors

Operational amplifiers of the 741 type are provided with both inverting and non-inverting input terminals, and can readily be used as differential amplifiers. Differential amplifiers give an output that is proportional to the difference between two input signals, i.e., to the value of one input minus the other, and such circuits are thus capable of carrying out the function of subtraction.

Figure 2.16 shows the practical circuit of a unity-gain differential d.c. amplifier or subtractor. The circuit functions as an inverting amplifier to one input, and as a non-inverting amplifier to the other. Looking first at the input-1 circuitry, it can be seen that if the input-2 terminal is grounded the $R_1 - R_2$ potential divider makes the op-amp work as a x 2 non-inverting amplifier, but the $R_3 - R_4$ potential divider causes only half of the input-1 signal to appear at the positive terminal of the op-amp, so that a non-inverted overall gain of unity takes place between the input-1 terminal and the output.

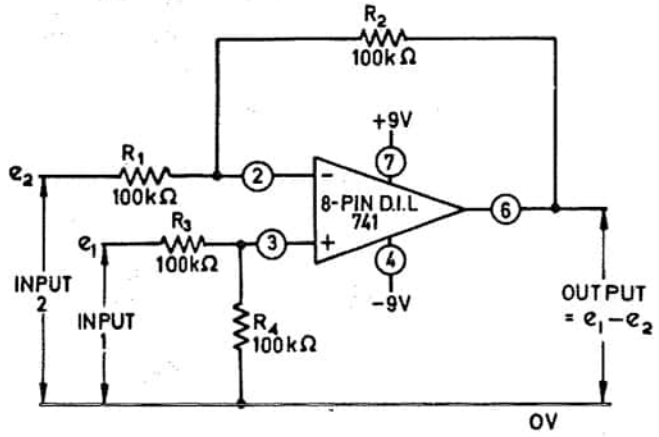


Figure 2.16. Unity-gain differential d.c. amplifier, or subtractor.

Looking now at the input-2 circuitry, it can be seen that the positive terminal is effectively grounded via R_4, and resistors R_1 and R_2 make the op-amp function as a unity-gain inverting amplifier. Thus, the circuit gives unity gain to both inputs, but the input-2 signal gives an inverted output, and the input-1 signal gives a non-inverted output. Consequently, the outputs tend to oppose each other, and the output is equal to input-1 minus input-2. The circuit can be used to carry out the function of subtraction.

The *Figure 2.16* circuit can, if required, be made to give voltage gain by suitably selecting the divider resistor values. The resistors can be given any values on condition that the ratio of R_1 to R_2 is the same as that of R_3 to R_4, in which case the voltage gain is equal to R_2/R_1. *Figure 2.17* shows suitable values for making a x 10 differential d.c. voltage amplifier or subtractor with gain.

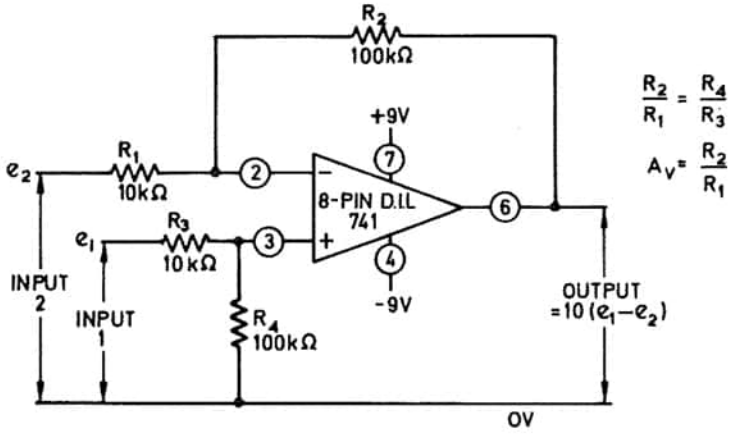


Figure 2.17. x 10 differential d.c. amplifier, or subtractor with gain.

Finally, *Figure 2.18* shows the connections for making a variable-gain differential d.c. amplifier, in which the gain can be varied from x 4 to x 22 via a single variable resistor. Here, resistors R_2 and R_4 are centre-tapped and are coupled via variable resistor R_5 and limiting resistor R_6. When R_5 is adjusted to a value of 0 Ω, the circuit gives a voltage gain of 22, and when R_5 has a value of 100 kΩ the gain falls to x 4.

The three differential amplifier circuits of *Figure 2.16* to *2.18* can be adapted for a.c. use by wiring blocking capacitors in series with each of their input terminals.

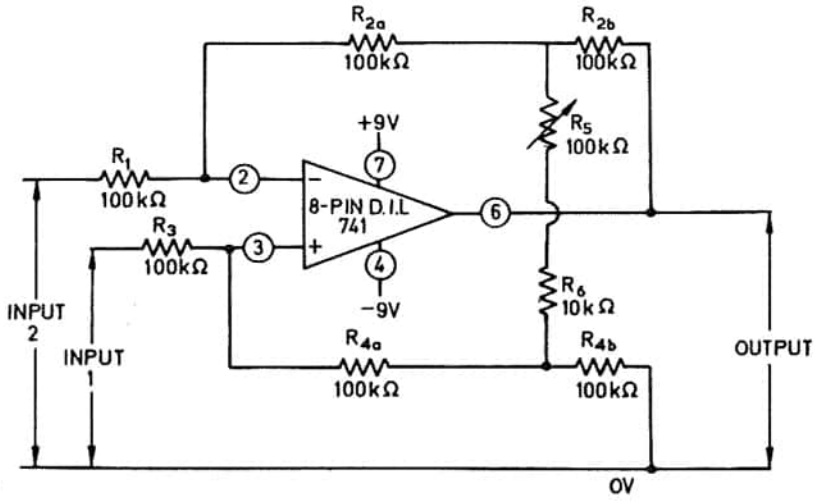
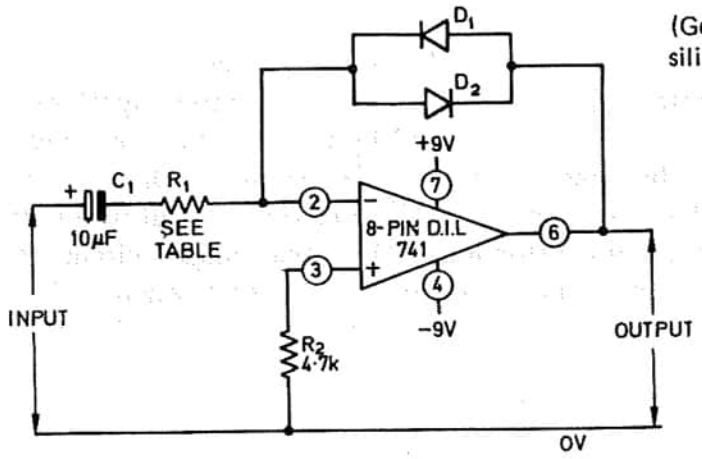


Figure 2.18. Variable-gain (x 4 to x 22) differential d.c. amplifier.

A non-linear (semi-log) amplifier

All the circuits that we have looked at so far in the chapter have been used to give linear voltage amplification, and have used simple resistive feedback elements. Op-amp circuits can be made to give non linear amplification by simply incorporating non-linear elements in their feedback paths. *Figure 2.19* shows a particularly useful type of non-linear amplifier. This circuit in fact gives a semi-log scale of voltage gain. This type of amplification is obtained because silicon diodes D_1 and D_2 are used as the negative feedback elements in an inverting amplifier circuit, and the forward current of a silicone diode varies in approximate proportion to the log of the applied diode voltage. With near-zero applied voltage the diodes act like very high resistances, so the circuit gain is high. With large applied voltages the diodes act like very low resistances, so the circuit gain is low.



INPUT VOLTS (R.M.S)	R_1 = 1kΩ		R_1 = 10kΩ	
	V_{OUT} (R.M.S)	GAIN	V_{OUT} (R.M.S)	GAIN
1 mV	110 mV	X 110	21 mV	X 21
10mV	330 mV	X33	170mV	X 17
100mV	450 mV	X4·5	360mV	X 3·6
1V	560 mV	X0·56	470mV	X 0·47
10V	600 mV	X0·07	560mV	X0·056

Figure 2.19. Circuit and performance table of non-linear (semi-log) a.c. voltage amplifier.

The table in *Figure 2.19* shows the measured circuit performance of the prototype amplifier when using two alternative values of input resistance. Using a 1 kΩ value of input resistance the circuit gives an r.m.s. output of 600 mV with a 10 V input, and a 330 mV output with an

input of 10 mV, i.e., a 1 000:1 change in input causes only a 2:1 change in output. The range of compression can be adjusted by using alternative values of R_1. It should be noted that this circuit gives an approximately square wave output when fed with a sine wave input.

This non-linear type of amplifier is particularly useful as an a.c. bridge-balance detector, in which case the output of the amplifier should be taken to the 1 V or 300 mV range of an a.c. millivolt-meter. The output of an a.c. measuring bridge varies over very wide limits between the balanced and unbalanced states, and it is necessary for the operator to frequently adjust the level of the output-level control in most instruments. If the bridge output is taken to the non-linear amplifier, however, this sensitivity adjustment can be eliminated, since the unit enables voltage level variations over a range of about 10 000:1 to be accommodated on a single range of a millivoltmeter.

Constant-volume amplifier circuits

The non-linear amplifier of *Figure 2.19* gives a virtually constant-amplitude output signal over a wide range of input signal levels, but achieves this constant-level output by introducing heavy amplitude distortion to the signal. In many applications it is desirable to have a circuit which gives a constant-amplitude output, but which does so without introducing distortion to the signal. Such a circuit can be built by using a self-adjusting voltage-controlled linear element in the negative feedback loop of an inverting amplifier. A circuit of this type is shown in *Figure 2.20a*.

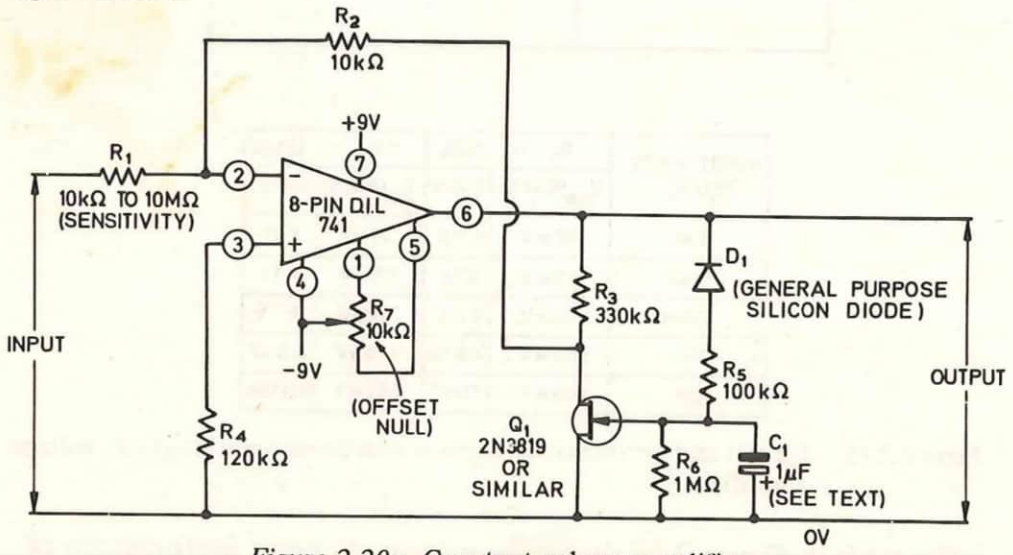


Figure 2.20a. Constant-volume amplifier.

In this circuit the op-amp is wired as an inverting d.c. amplifier, with its gain controlled by the potential divider formed by R_3 and field-effect

transitor Q_1. In this particular application the f.e.t. is used as a voltage-controlled resistor, the control bias voltage being obtained from the op-amp output via $D_1 - R_5 - R_6$ and C_1. With zero bias applied to Q_1 gate the f.e.t. acts like a resistance of a few hundred ohms; with a large negative bias applied to the gate the f.e.t. acts like an open circuit.

Thus, when a low-amplitude signal is applied to the op-amp input a small signal voltage tends to appear at the op-amp output. Under this condition very little negative bias is developed at the f.e.t. gate, so the f.e.t. acts like a resistance of only a few hundred ohms. The potential divider action of R_3 and Q_1 results in very little negative feedback under this condition, so the circuit gives a very high voltage gain and tends to increase the op-amp output signal to a reasonable level.

When a large-amplitude signal is applied to the op-amp input, on the other hand, a large signal voltage tends to appear at the op-amp output. Under this condition a large negative bias is developed at the f.e.t. gate, so the f.e.t. acts like an open circuit. Negligible voltage divider action takes place between R_3 and Q_1 under this condition, so heavy negative feedback is applied to the op-amp via R_3, and the circuit gives a very low voltage gain and tends to reduce the op-amp output signal to a reasonable level. Self-regulation of the signal output level thus takes place, and does so without introducing appreciable distortion to the signal.

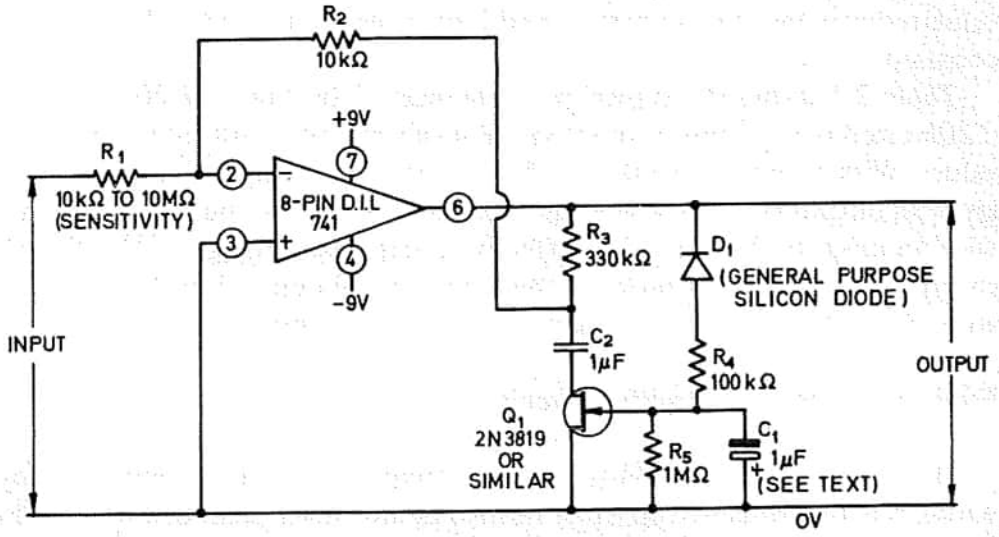


Figure 2.20b. Improved constant-volume amplifier.

In practice the *Figure 2.20a* circuit is capable of giving a virtually constant-amplitude output signal over a 30 dB range of input signal levels, the actual signal operating range being determined by R_1. R_1 is selected to handle the *maximum* input signal required, since the output becomes distorted when this level is exceeded.

A minor snag of the *Figure 2.20a* circuit is that it has an inherently

poor d.c. stability, and requires the use of offset null control R_7 to compensate for this defect. The poor d.c. stability occurs because negligible d.c. negative feedback takes place under low-level input conditions, when the f.e.t. is acting as a low resistance and the circuit is giving a very high gain. This snag can be overcome, and the need for an offset null control eliminated, by wiring a blocking capacitor between the drain of Q_1 and the $R_2 - R_3$ junction, as shown in the improved constant-volume amplifier circuit of *Figure 2.20b.* The capacitor acts as an open circuit to d.c., so a high degree of d.c. negative feedback is applied to the op-amp via R_2 and R_3, and the circuit has good d.c. stability. The capacitor acts as a short circuit to a.c. at normal operating frequencies, however, so the voltage divider action of R_3 and Q_1 is unimpaired and the circuit acts as a constant-volume amplifier to a.c. signals.

The *Figure 2.20a* and *2.20b* circuits give virtually identical performances. In both cases R_1 determines the signal operating range of the circuit, and is selected to suit the *maximum* input signal that the circuit is expected to handle. The R_1 value is selected on the basis of 200 kΩ/V of r.m.s. input signal: for a maximum input of 50 V R_1 is given a value of 10 MΩ, and for a maximum input of 50 mV R_1 is given a value of 10 kΩ. Capacitor C_1 determines the 'follow' or a.g.c. time constant of the circuit, and its value can be changed to suit individual needs: reducing the C_1 value reduces the time constant, and increasing C_1 increases the time constant.

Table 2.1 shows the typical performance of the *Figure 2.20 a* and *2.20b* circuits at different input signal levels and with alternative R_1 values. With R_1 given a value of 1 MΩ (to suit a 5 V input), the circuit gives an output of 2.85 V with an input of 5 V, and an ouput of 1.48 V with an input of 100 mV. The effective compression range of the circuit is roughly 30 dB. Two or more of these constant-volume circuits can be wired in series, if required, to give even greater compression.

Frequency-selective amplifier circuits

Op-amps can be made to function as frequency-selective amplifiers by wiring reactive resistor-capacitor networks into their feedback loops. They can be made to act as frequency-selective tuned amplifiers or acceptor filters, as notch or rejector filters, or as high pass or low-pass amplifiers, etc. Five useful frequency-selective circuits are shown in this final section of this chapter.

Figure 2.21 shows the practical circuit of a 1 kHz frequency-selective tuned amplifier or acceptor filter. The circuit exhibits characteristics similar to those of an *LC* tuned amplifier with a Q of about 50. The circuit gives a gain of x 200 to signals at the centre frequency of 1 kHz,

Table 2.1 Performance results for the *Figure 2.20a* and *b* circuits.

V_{IN} (R_1 = 10KΩ)	V_{IN} (R_1 = 100KΩ)	V_{IN} (R_1 = 1MΩ)	V_{IN} (R_1 = 10MΩ)	V_{OUT}
50 mV	500 mV	5 V	50 V	2.85 V
20 mV	200 mV	2 V	20 V	2.81 V
10 mV	100 mV	1 V	10 V	2.79 V
5 mV	50 mV	500 mV	5 V	2.60 V
2 mV	20 mV	200 mV	2 V	2.03 V
1 mV	10 mV	100 mV	1 V	1.48 V
500 μV	5 mV	50 mV	500 mV	0.89 V
200 μV	2 mV	20 mV	200 mV	0.40 V
100 μV	1 mV	10 mV	100 mV	0.20 V
50 μV	500 μV	5 mV	50 mV	0.10 V

but at 500 Hz (one octave down) the gain is roughly x 3, and at 2 kHz (one octave up) the gain is roughly x 2. The gain falls to unity at 150 Hz and 3.3 kHz.

The operating theory of the *Figure 2.21* circuit is quite simple. The op-amp is wired as an inverting amplifier with twin-T filter $R_2 - R_3 - R_4$ and $C_2 - C_3 - C_4$ wired in the negative feedback loop between the output and the negative input terminal. In this application the twin-T filter acts like a frequency-controlled resistor that presents a near-infinite

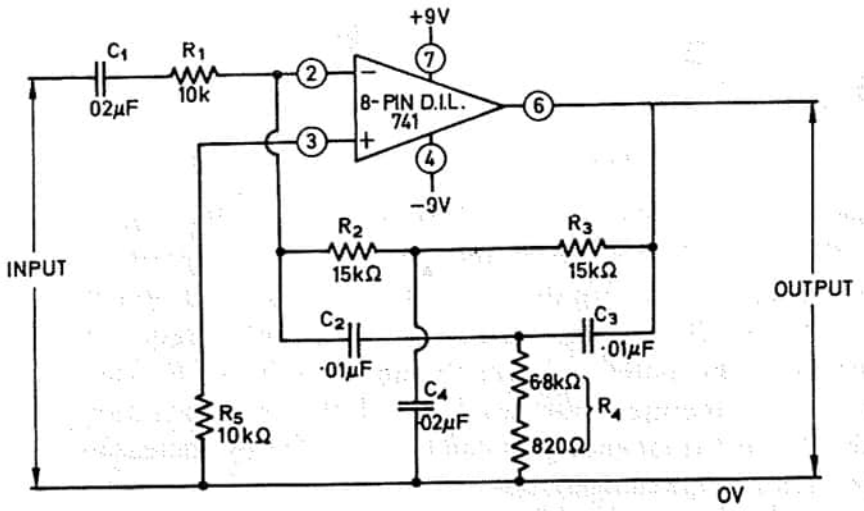


Figure 2.21. 1 kHz tuned (acceptor) amplifier (twin-T).

impedance at the centre frequency, but a low impedance at all other frequencies. Consequently, at the centre frequency negligible negative feedback is applied to the circuit, and very high gain is available, but at

all other frequencies heavy negative feedback is applied, and the gain is low.

The centre frequency of the circuit is determined by the twin-T component values, and these can be changed to satisfy individual requirements. The twin-T resistors should ideally be kept in the ratios $R_2 = R_3 = 2 \times R_4$, and the twin-T capacitors must be kept in the ratios $C_2 = C_3 = C_4/2$, in which case the centre frequency of the circuit $= 1/6.28\, R_2.C_2$. In practice the stability of the circuit is enhanced by making R_2 and R_3 very slightly greater than $2 \times R_4$ (by about 2 %). The C_1 input capacitor value of the design is selected to improve the low-frequency rejection of the circuit, and should be given the same value as C_4.

Figure 2.22 shows how the *Figure 2.21* circuit can be changed into a 1 kHz notch or rejector circuit by repositioning the twin-T filter. This circuit totally rejects input signals at the centre frequency of 1 kHz, but accepts and gives unity gain to all other input signals. The centre

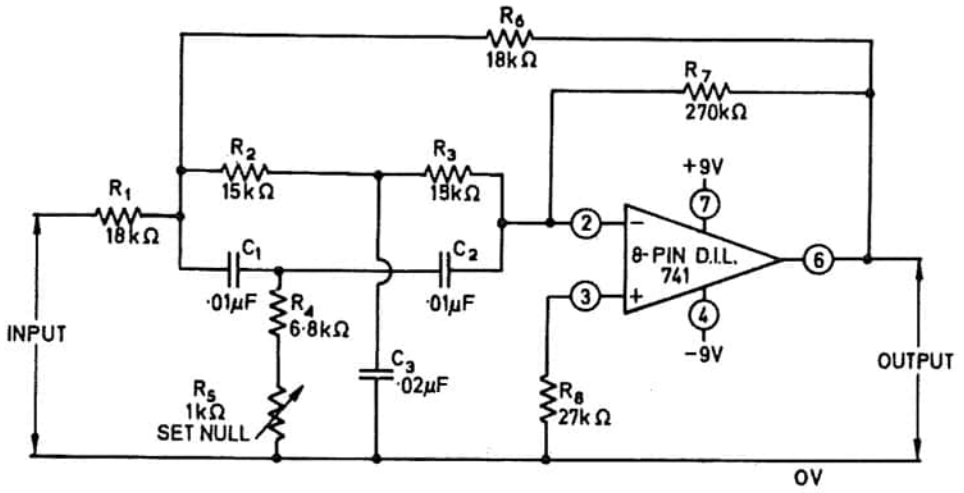


Figure 2.22. 1 kHz notch (reject) filter.

frequency is controlled by twin–T network $R_2 - R_3 - R_4 - R_5$ and $C_1 - C_2 - C_3$. The rejector notch can be made exceptionally narrow by adjusting R_5; once set up the circuit gives negligible attenuation to signals that are 20 % or more away from the centre frequency. The notch sharpness can be increased by increasing the value of R_7 (up to 1 MΩ maximum), if required, but a perfect null then becomes more difficult to obtain. The off-frequency gain can be increased by increasing the value of R_6 (to 1.8 MΩ maximum), but this increase in gain is obtained at the expense of reduced notch sharpness.

The two frequency-selective circuits that we have looked at so far have both used twin-T filters as their frequency-selecting elements. Other types of *RC* frequency-selecting networks can also be used in op-amp circuits. *Figure 2.23*, for example, shows how a Wien network

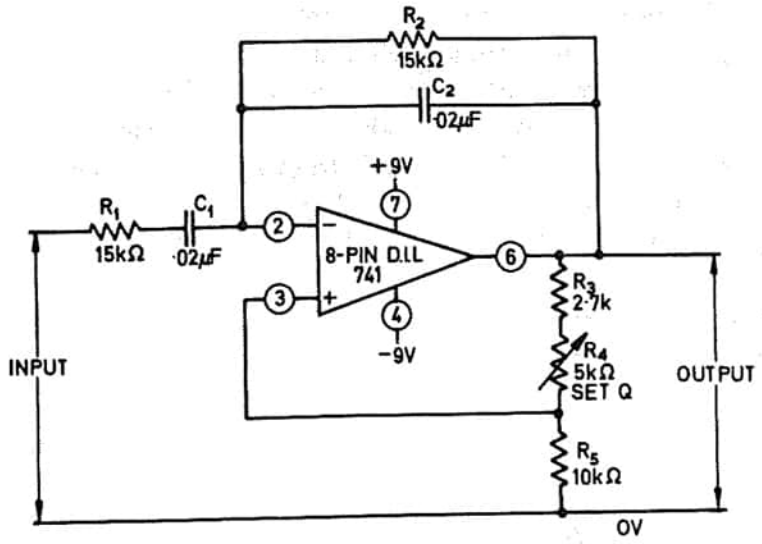


Figure 2.23. 1 kHz tuned (acceptor) amplifier (Wien).

($R_1 - R_2 - C_1 - C_2$) can be connected to an op-amp so that it functions as a 1 kHz frequency-selective tuned amplifier or acceptor filter.

This circuit employs two feedback paths. One path is from the output to the negative input terminal of the op-amp via the Wien network, and the other is from the output to the positive input terminal via the $R_3 - R_4$ and R_5 potential divider. The circuit action is such that the two feedback signals cancel each other out at the Wien centre frequency, so the circuit gives very high gain to centre-frequency signals. At all other frequencies the two signals do not self-cancel, so the circuit gives low gain to all off-tune frequencies.

Ideally, R_5 should have a value exactly double the sum of R_3 and R_4; slight errors in these ratios result in either oscillation (R_5 value too large) or very low effective Q (R_5 value too small). R_4 is used to set the circuit Q or tuning sharpness to an acceptable level, consistent with good circuit stability. The centre frequency of the circuit can be made variable by replacing R_1 and R_2 with a two-gang variable resistor.

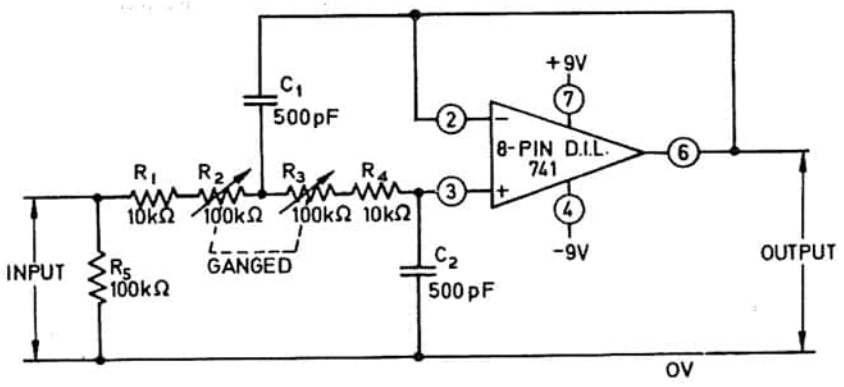


Figure 2.24. Variable low-pass filter, covering 2.2 kHz to 24 kHz.

Figure 2.24 shows the circuit of a variable low-pass filter. This circuit gives unity gain to all frequencies below a certain cut-off value, but attenuates all signals above the cut-off frequency. The cut-off frequency is defined here as the frequency at which the output signal falls by 3 dB relative to the input signal. The cut-off frequency of the circuit can be varied via the two-gang $R_2 - R_3$ variable resistor from 2.2 kHz ($R_2 = R_3 = 100\ \text{k}\Omega$) to 24 kHz ($R_2 = R_3 = 0\ \Omega$). Beyond the cut-off frequency the circuit exhibits a 2nd order response in which the gain falls by 12 dB for each octave increase in frequency, or by 40 dB for each decade increase in frequency.

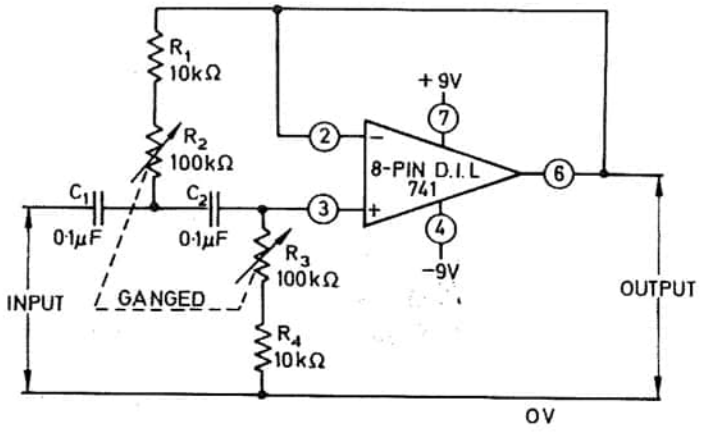


Figure 2.25. Variable high-pass filter, covering 235 Hz to 2.8 kHz.

Finally, *Figure 2.25* shows the circuit of a variable high-pass filter. This circuit gives unity gain to all frequencies above a certain cut-off value, but attenuates all signals below the cut-off frequency. The cut-off frequency is again defined as the frequency at which the output signal falls by 3 dB relative to the input signal, and can be varied via R_2 and R_3. The cut-off frequency is variable from 235 Hz ($R_2 = R_3 = 100\ \text{k}\Omega$) to 2.8 kHz ($R_2 = R_3 = 0\ \Omega$). Beyond the cut-off point the circuit has a 2nd order response in which the gain falls by 12 dB for each octave decrease in frequency, or by 40 dB for each decade decrease in frequency.