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Using MOS FET Integrated Circuits in Linear Circuit Applications

by S. Reich

Although the discrete metal-oxide-semiconductor (MOS) field-effect transistor (FET) has been available for many years,[1] its usage has been comparatively limited. Designers have been reluctant to employ MOS FET devices in their circuits because the gate oxide in a discrete device is vulnerable to damage by static electricity discharges encountered during handling and/or electrical transients found in circuit applications. RCA engineers have now successfully combined MOS FET and integrated-circuit (IC) fabrication techniques to produce a simple monolithic MOS FET IC in which back-to-back diodes are connected in shunt with the gate oxide to restrict the gate potential appearing across the gate oxide. The simple gate-protected IC's are of major significance because their immunity to damage by static electricity or by in-circuit transients is on a par of excellence with that of other solid-state devices intended for similar types of applications. Consequently, circuit designers can now practically utilize the many unique MOS FET characteristics, viz., high input impedance, square-law transfer characteristic, wide dynamic range, dual-gate configuration, etc. For example, the square-law transfer characteristic is especially desirable in the maintenance of low cross-modulation characteristics in rf amplifiers.[2,3] This paper contains a brief review of the device theory, followed by a survey of some linear circuit applications for the MOS FET IC.

REVIEW OF DEVICE THEORY

The operating voltage applied to the MOS FET determines whether the device will function as a resistor, an amplifier, or a diode. This section will provide a review of these various MOS FET operational modes. Subsequently, the useful operational modes will be employed in typical applications.

Fig. 1 is a sketch, for zero gate-to-source voltage, of I_D as a function of V_{DS} for an n-channel depletion-type MOS FET. Changes in the conductivity pattern are shown in the simplified conductivity profile for each region of operation.

Ohmic – Region 'A' depicts an I_D-V_{DS} curve that is characteristic of a resistance. The shape of this curve is a function of V_{DS} (drain-to-source voltage). Its slope is governed by V_{GS} (gate-to-source voltage). The V_{DS}/I_D characteristic i.e., its resistance value, is controlled by the gate voltage.

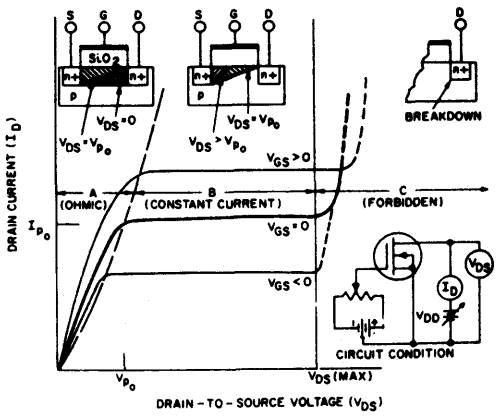


Fig. 1–Regions of operation – n-channel depletion MOS FET.

As V_{DS} is increased, it produces an electrostatic stress in the channel that modifies the channel conductivity as shown. The channel is completely pinched off beyond V_{Po} (pinch-off voltage). Increasing V_{DS} serves only to maintain I_D at a constant level.

Amplifier[4] – For a fixed gate-voltage, I_D is at a constant level in region 'B'. A change in V_{GS} produces a change in I_D; thus in region 'B' the device exhibits the transconductance characteristic that is essential in amplifier operation (i.e., $G_m = dI_D/dV_{GS}$).

"Forbidden" Region – Increase of V_{DS} beyond its rated maximum could produce avalanching in the drain-to-substrate diffusion (diode). Therefore MOS FET devices should not be operated in this region.

The dual-gate device is a serial arrangement of two single-gate devices. This arrangement improves the MOS FET performance by reducing capacitance from output to input (drain to gate 1), and provides an added control element that adds to the versatility of the MOS FET.

Gate Protection

A gate-protection system, which can be incorporated as an integral part of the transistor structure, has been developed for dual-gate MOS transistors. In devices that include this protection system, a set of back-to-back diodes is fabricated on the semiconductor pellet and connected between each insulated gate and the source. (The low junction-capacitance of the small diodes represents a relatively insignificant addition to the total capacitance that shunts the gate.) Fig. 2 is a profile drawing and schematic symbol for an n-channel dual-gate-protected depletion-type MOS field-effect transistor. The MOS FET IC metallization pattern, including the connections to the drain, gate 1, gate 2, source, and protective devices, all on a single monolithic structure, is shown in Figure 3.

The back-to-back diodes do not conduct unless the gate-to-source voltage exceeds typically ±10 volts. The transistor, therefore, can handle a very wide dynamic signal swing without significant conductive shunting effects by the diodes (leakage through the "nonconductive" diodes is very low, typically 1 na). If the potential on either gate exceeds typically +10 volts, the upper diode (shown in Fig. 2) of the pair associated with that particular gate becomes conductive in the forward direction and the lower diode breaks down in the backward (Zener) direction. In this way, the back-to-back diode pair provides a path to shunt excessive positive charge from the gate to the source. Similarly, if the potential on either gate exceeds typically -10 volts, the lower diode becomes conductive in the forward direction and the upper diode breaks down in the reverse direction to provide a shunt path for excessive negative charge from the gate to the source. The diode gate-protection technique is described in more detail in the following section on integrated gate protection.

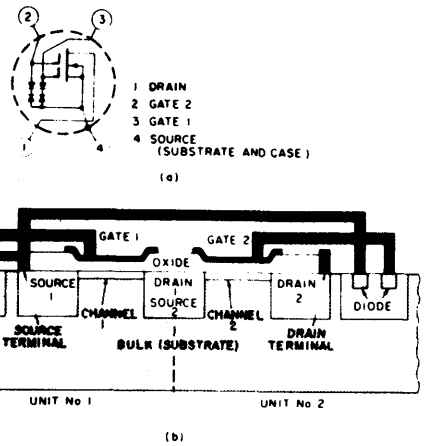


Fig. 2–Protected dual-gate MOS FET IC: (a) schematic diagram; (b) profile sketch.

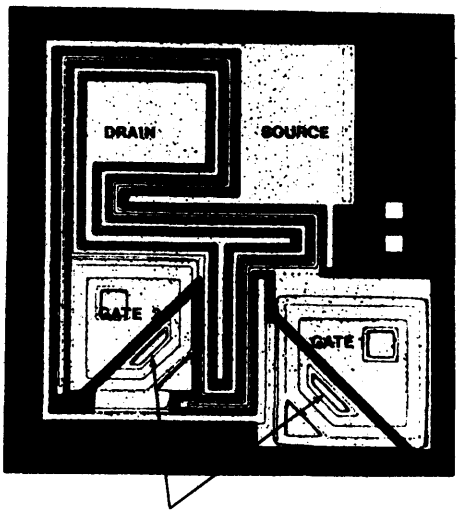


Fig. 3–Monolithic protected dual-gate MOS FET IC.

Integrated Gate Protection

The advent of an integrated system of gate-protection in MOS field-effect transistors has resulted in a class of solid-state devices that exhibits ruggedness on a par with other solid-state rf devices. The gate-protection system mentioned in the preceding section offers protection against static discharge during handling operations without the need for external shorting mechanisms. This system also guards against potential damage from in-circuit transients. Because the integral gate-protection system has provided a major impact on the acceptability of MOS field-effect transistors for a broad spectrum of applications, it is pertinent to examine the rudiments of this system.

Fig. 4 shows a simple equivalent circuit for a source of static electricity that can deliver a potential e_O to the gate input of an MOS transistor. The static potential E_S stored in

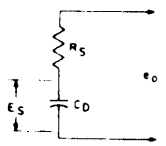


Fig. 4–Equivalent circuit for source of static electricity.

an "equivalent" capacitor C_D must be discharged through an internal generator resistance R_S. Laboratory experiments indicate that the human body acts as a static (storage) source with a capacitance C_D ranging from 100 to 200 picofarads and a resistance R_S greater than 1000 ohms. Although the upper limits of accumulated static voltage can be very high, measurements suggest that the potential stored by the human body is usually less than 1000 volts. Experience has also indicated that the likelihood of damage to an MOS transistor as a result of static discharge is greater during handling than when the device is installed in a typical circuit. In an rf application, for example, static potential discharged into the antenna must traverse an input circuit that normally provides a large degree of attenuation to the static surge before it appears at the gate terminal of the MOS transistor. The ideal gate-protection signal-limiting circuit is a configuration that allows for a signal, such as that shown in Fig. 5(a), to be handled without clipping or distortion, but limits the amplitude of all transients that exceed a safe operating level, as shown in Fig. 5(b). An arrangement of back-to-back diodes, shown in Fig. 5(c), meets these requirements for protecting the gate insulation in MOS transistors.

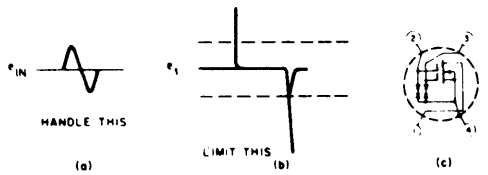


Fig. 5—Gate-protection requirements and solution.

Ideally, the transfer characteristic of the protective signal-limiting diodes should have an infinite slope at limiting, as shown in Fig. 6(a). Under these conditions, the static potential across C_D in Fig. 6(b) discharges through its internal impedance R_S into the load represented by the signal-limiting diodes. The ideal signal-limiting diodes, which have an infinite transfer slope, would then limit the voltage present at the gate terminal to its knee value, e_d. The difference voltage e_S appears as an IR drop across the internal impedance of the source R_S, i.e., $e_S = E_S - e_d$ where E_S is the potential in the source of static electricity and e_d is the diode voltage drop. The instantaneous value of the diode current is then equal to e_S/R_S. During physical handling, practical peak values of currents produced by static-electricity discharges range from several milliamperes to several hundred milliamperes.

Fig. 7 shows a typical transfer characteristic curve measured on a typical set of back-to-back diodes used to protect the gate insulation in an MOS field-effect transistor that is nominally rated for a gate-to-source breakdown

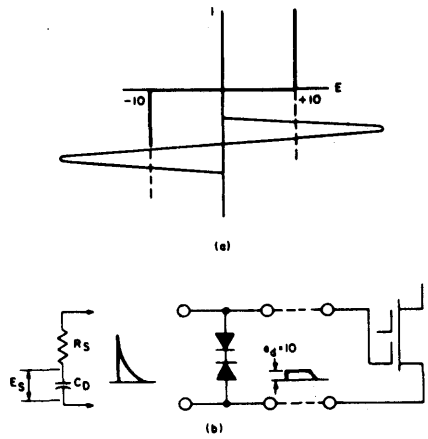


Fig. 6—Ideal transfer characteristic of protective diodes (a), and resulting waveforms in equivalent circuit (b).

voltage of 20 volts. The transfer-characteristic curves show that the diodes will constrain a transient impulse to potential values well below the ±20 volt limit, even when the source of the transient surge is capable of delivering several hundred milliamperes of current. (These data were measured with 1-microsecond pulses applied to the protected gate at a duty factor of 4×10^{-3}).

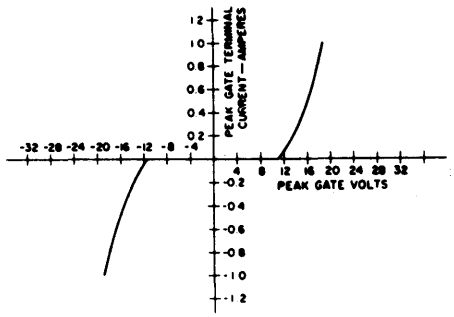


Fig. 7—Typical diode transfer characteristic.

Electrical Requirements

The previous discussion points out that optimum protection is afforded to the gate with a signal-limiting diode that exhibits zero resistance (i.e., an infinite transfer slope and fast turn-on time) to all high-level transients. In addition, the ideal diode adds no capacitance or loading to the rf input circuit. This ideal diode in practice simply does not exist, but integrated circuit techniques made possible the development of a gate-protected MOS FET IC that is close to the ideal. For example, Fig. 8 shows typical 200-MHz input characteristic changes brought about by the addition of the integrated circuit diodes. Their effect on power gain and noise factor is shown by the data given in Table I. These data indicate that there are no discernible reductions in power gain and a trivial noise factor increase of about 0.25 dB.

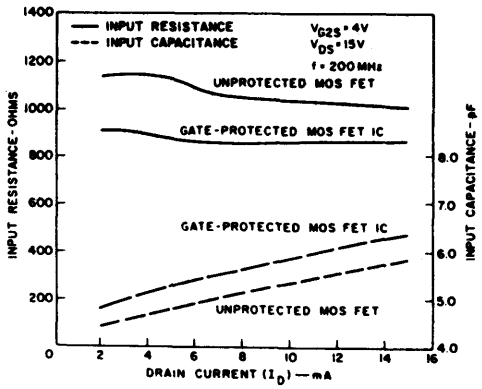


Fig. 8—Input resistance and capacitance as functions of drain current for the MOS FET with and without diodes.

Table I - Power Gain and Noise Factor at 200 MHz

UNIT	POWER GAIN (dB)		NOISE FACTOR (dB)	
	DIODES IN	DIODES REMOVED	DIODES IN	DIODES REMOVED
1	16.3	16.4	3.7	3.4
2	18.8	18.5	2.4	2.2
3	16.5	16.2	3.3	3.0
4	16.3	15.7	3.9	3.4
5	17.7	17.8	2.6	2.4
6	17.2	17.5	2.8	2.5
7	17.1	17.0	3.3	3.2
8	17.9	18.0	2.9	2.6
9	18.5	18.5	2.4	2.3
10	17.3	17.3	3.2	3.0

The Triode-Connected Protected Dual-Gate IC

The dual-gate MOS FET can be connected so that it functions as a single-gate device, as shown in Fig. 9. The triode-connected configuration has curve tracer (drain family) characteristics that look like the 'real' triode. The curves in Fig. 10 show that characteristics for the triode MOS FET (3N128) and the triode-connected dual-gate MOS FET (3N187) are essentially similar.

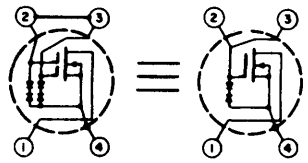


Fig. 9—Dual-gate MOS FET IC in a single-gate configuration.

Triode-Connected-Device Characteristics

Some useful triode-connected-device characteristics are provided in Table II in the form of comparisons with dual-gate and single-gate devices. It should be noted that the difference in I_{DS} level between the 3N187 and the 3N200 carries over to their triode-connected versions. A curve showing I_{DSS} for triode connection versus I_{DS} for the dual-gate configuration (i.e., V_{G2S} = 4 volts) is shown in Fig. 11.

A plot of the triode-connected dual-gate transfer characteristics (I_D vs. V_{GS}) is shown in Fig. 12; similarly, g_{fs} curves are given in Fig. 13 as functions of I_D. Curves for typical dual-gate operation are available in commercial data sheets.[5,6]

Dual gates connected as tetrodes and triodes were evaluated for $R_{D(ON)}$ where 'on' resistance compares favorably with single-gate devices. Typical variations in $R_{D(ON)}$ as a function of gate voltage are shown in Fig. 14.

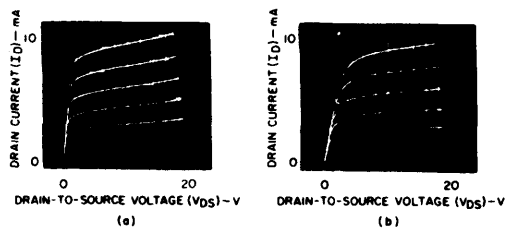


Fig. 10—Drain families: (a) for triode-connected protected dual-gate device; (b) for triode.

Table II – Comparison of Typical Electrical Characteristics for Triode-Connected Dual-Gate, Dual-Gate, and Triode MOS FET Devices

CHARACTERISTIC	CONDITIONS	TRIODE–CONNECTED		DUAL–GATE CIRCUIT*		SINGLE GATE	UNITS
		3N187	3N200	3N187	3N200	3N128	
I_{DS}	V_{DS} = 15 v	6.0	2.0	15	5	15	mA
g_{fs}	V_{DS} = 15 v, I_D = 10 mA, f = 1 kHz	7.0	8.5	12	15	9	mmho
$V_{G1S(OFF)}$	V_{DS} = 15 v, I_D = 50 μA	-2.0	-1.0	-2.0	-1.0	-1.5	V
I_{G1SS}	V_{GS} = ±6 v	2.0	2.0	1.0	1.0	10^{-4}	nA
C_{iss}	V_{DS} = 15 v, I_D = 10 mA, f = 1 kHz	10.0	10.0	6.0	6.0	5.5	pF
C_{rss}	V_{DS} = 15 v, I_D = 10 mA, f = 1 kHz	0.5	0.5	0.02	0.02	0.2	pF
C_{oss}	V_{DS} = 15 v, I_D = 10 mA, f = 1 kHz	2.0	2.0	2.0	2.0	1.4	pF
$R_{DS(ON)}$	V_{DS} = 1 v, V_{GS} = 0	160	250	100	150	300	ohm

*V_{G2S} = 4 v except for I_{GSS} measurement, where V_{G2S} = 0.

It should not be inferred from these comments that all single-gate applications can be handled by the protected dual-gate device. The advent of MOS FET opened application areas in which circuit requirements imposed leakage-current limits in the picoampere range. For these applications the present generation of protective gate devices do not suffice and it is necessary to employ a "classical" MOS FET type (e.g., 3N128) and exercise precautions against gate-insulation puncture.

SURVEY OF LINEAR APPLICATIONS

This section shows typical circuit arrangements. Some are documented, and others are design ideas for use of dual-gate MOS FET's with integrated diodes in applications using tetrode and triode-connected configurations.

Choppers

The circuits shown in Fig. 15 use the dual-gate MOS FET IC in chopper or gating circuits. In the shunt-circuit configurations shown in Figs. 15(a) and 15(b), the MOS device is normally conductive, i.e., e_o is low. A negative gating-pulse turns off the MOS device so that approximately 50 percent of e_g appears at the output terminals. Circuit (a) features the use of an additional control potential (V_{G2}). A dc potential may be applied as shown to the second gate, thereby establishing the value of desired channel 'on' resistance (R_{DS}). Alternatively, circuitry can be arranged so that the second gate can function as a "coincidence-gate", i.e., to reduce e_o to a low value, a positive-going pulse must be applied to gate 2 simultaneously with a positive-pulse to gate 1.

All circuits in Fig. 15 make reference to Note (A). The circuit diagrams show a "jumper" connected between two terminals in the drain-to-ground-return circuits. The circuits as drawn assume a peak generator level (e_g) of less than 0.2 volts. Should the signal exceed this value, it is possible that the "n-p" parasitic diode between the drain and semi-

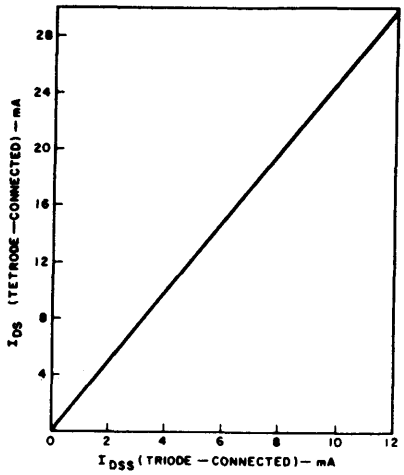


Fig. 11—Correlation of zero-bias drain current for the protected dual-gate device in tetrode (I_{DS}) and triode (I_{DSS}) configurations.

conductor substrate will be driven into conduction and load the signal. This contingency may be obviated (with a simultaneous improvement in attenuator linearity) by connecting a suitable dc potential in lieu of the "jumper", so that a positive potential is applied to the drain. The magnitude of this voltage should equal or exceed the peak value of the rms signal from e_g.

Circuits shown in Figs. 15(c) and 15(d) function in a manner opposite to those described above, i.e., output voltage appears at e_o in the absence of a gating signal. Consequently, a negative gating signal reduces the level of e_o. The dual-gate configuration can be made into an 'or' circuit, i.e., a negative signal applied to gate 2 of sufficient magnitude to override V_{G2} will also reduce the level at e_o.

Attenuators

Fig. 16 shows the dual-gate device in an attenuator circuit. In Fig. 16(a) both gates are used as control elements. This type of circuitry is particularly attractive when control of the attenuator must be located at some remote location. A dc potential on gate 1 has greater control on the channel resistance than is the case for gate 2. Thus an arrangement can be used whereby gate 2 provides a "fine" attenuator adjustment and gate 1 controls "course" adjustment. The circuit in Fig. 16(b) shows the dual-gate device in a triode-connected attenuator circuit. Curves showing typical variations in resistance as a function of gate-voltage were given in Fig. 14.

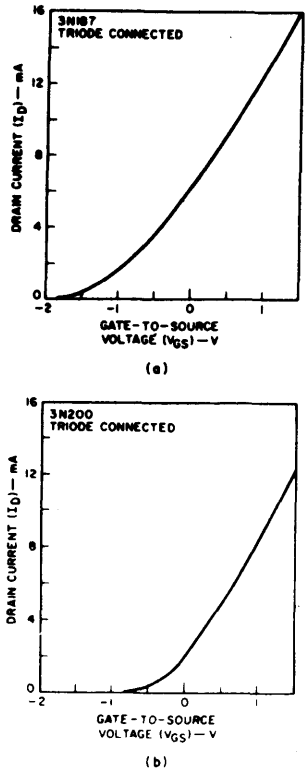


Fig. 12—Triode-connected protected dual-gate MOS FET IC transfer characteristics.

Constant-Current Sources

The characteristics of the MOS FET IC in the region beyond pinch-off make the device suitable for constant-current supplies, as illustrated in Fig. 17 (using a "triode-connected" dual-gate device).

The dual-gate device may be used to obtain higher values of current-regulation with the circuit depicted in Fig. 18. A supply circuit with a maximum output voltage capability of about 4.0 to 5.0 volts is required for V_{G2}. Values greater than this will have negligible effect on output current control.

The circuits in Fig. 19 use the MOS FET constant-current characteristic to make a regulated constant-voltage reference source by feeding I_{DS} through a fixed-value resistor.

In any typical amplifier application using the MOS FET device, e.g., in Fig. 20, the voltage developed across a bypassed source resistance provides a well-regulated fixed reference voltage (if the amplifier stage is not subjected to

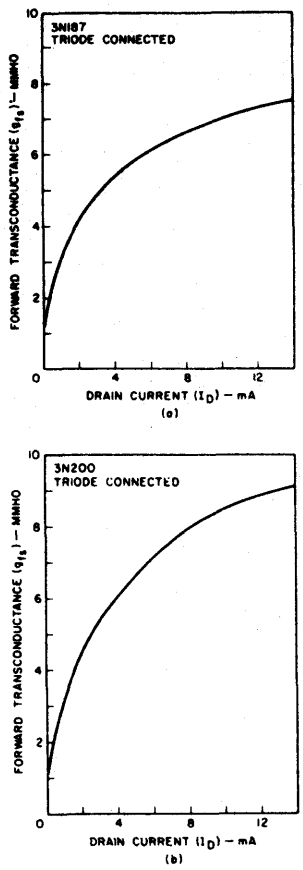


Fig. 13—Triode-connected protected dual-gate MOS FET IC transconductance characteristics.

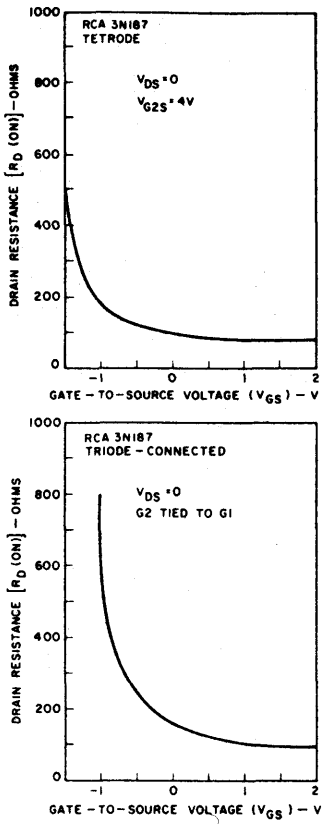


Fig. 14—"ON" resistance as a function of gate voltage for tetrode- and triode-connected protected dual-gate MOS FET IC's.

varying bias conditions, such as those encountered in connection with AGC). When a reference voltage is obtained in this manner, it is advisable to feed it to other circuitry through an adequate decoupling network.

General-Purpose Amplifier Circuits

Fig. 21 shows three basic single-stage amplifier configurations that utilize dual-gate-protected MOS FET IC's as triodes and as tetrodes in common source, common-drain, and common-gate circuits. Each configuration has its own particular advantages for specific applications. The dual-gate device has an added advantage in any of these configurations in that gate 2 provides (a) reduced gate-to-drain capacity by an order of magnitude, and (b) a convenient means for controlling the gain of the stage by adjusting the dc potential applied to gate 2.

A dual-gate device is shown in Fig. 22 as a shunt-type attenuator to control the input level to a source-follower. The source-follower uses the dual-gate MOS FET with gate 2 available as a control for adjusting the gain of the source-follower. The jumper in the ground return path of the generator can be used to insert a positive voltage on the drain for the reasons explained above.

Fig. 23 shows a circuit using the "triode-connected" dual-gate device in a simple 20-dB preamplifier for extending the sensitivity range of an oscilloscope or ac voltmeter. It can also be used in audio circuits as a phono preamplifier or microphone preamplifier. It is shown as self-contained, i.e.,

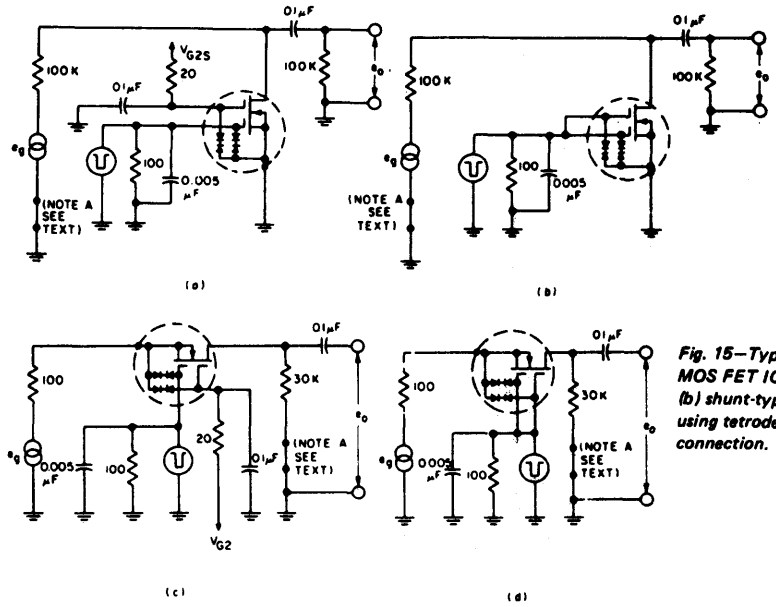


Fig. 15—Typical chopper circuits using protected dual-gate MOS FET IC's. (a) shunt-type using tetrode connection; (b) shunt-type using triode connection; (c) series-type using tetrode connection; (d) series-type using triode connection.

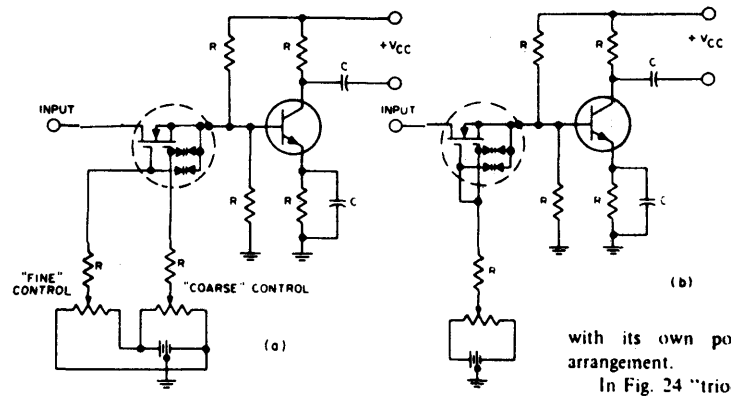


Fig. 16—Attenuator circuits using the protected dual-gate MOS FET IC: (a) variable series-type attenuator with coarse and fine controls; (b) variable series-type attenuator using triode-connected configuration.

with its own power supply and a by-pass switching arrangement.

In Fig. 24 "triode-connected" MOS FET devices are used in a simple differential amplifier configuration in which the "triode-connected" gates of the two devices are biased from a single source (the junction of R1 and R2). This arrangement is possible because the 3N187 has a typical gate current (I_{GSS}) in the triode configuration of 2 nanoamperes. Therefore, the bias can be supplied through R3 with a negligible voltage offset. Resistor R5 is used to null out the effects of slight differences in device characteristics so that the offset-voltage at e_o can be set to zero.

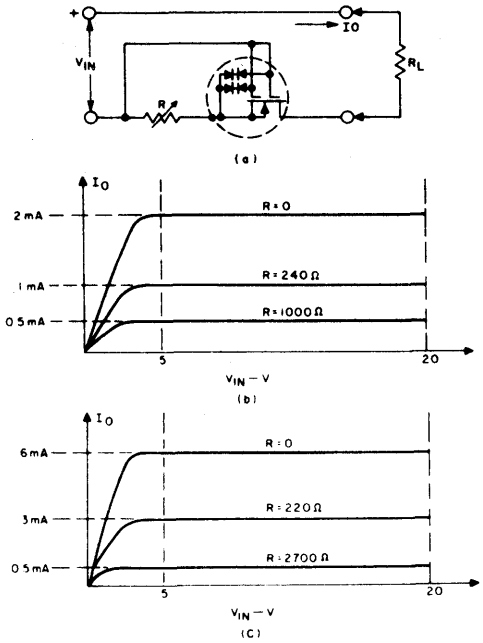


Fig. 17—Constant-current supply using protected dual-gate MOS FET IC in triode configuration: (a) basic circuit; (b) typical I_o vs. V_{in} for RCA-3N200 in the basic circuit; (c) typical I_o vs. V_{in} for RCA-3N187 in the basic circuit.

The circuit in Fig. 25 shows another differential amplifier configuration, in which the offset voltage at e_O can be set to zero by means of appropriate potentials supplied to the No. 2 gates, adjustment being provided by R6.

The circuit shown in Fig. 26 is a frequency-selective amplifier intended for operation within the audio frequency range of 10 Hz to 20 kHz. Frequency-selective circuits are used for selective coding, i.e., in garage-door openers, narrowing the bandwidth response in CW receivers to

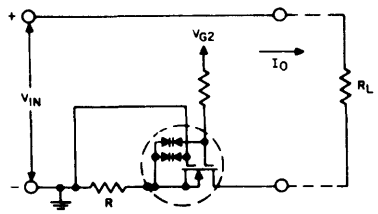


Fig. 18—Protected dual-gate device as a constant-current source.

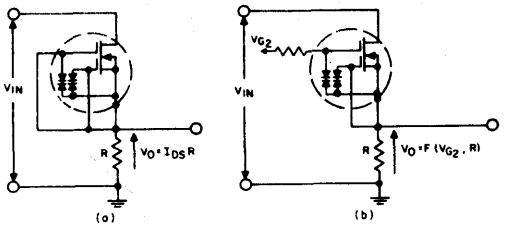


Fig. 19—Voltage-reference circuits using protected dual-gate MOS FET IC: (a) as triode; (b) as tetrode.

eliminate unwanted side bands, and in systems requiring some form of keying impulse (e.g., synchronizing the narration in a tape recorder with slides).

The frequency-selective circuit shown is an audio amplifier with a twin-"T" RC filter circuit in its output. This network provides regenerative feedback to the input circuit at an audio frequency predetermined by the selection of capacitors C5, C6, and C7. The peaking control R7 fine-tunes the twin-"T" for the desired frequency of operation, and potentiometer R8 adjusts the level of feedback for desired performance. The circuit as shown in Fig. 26 is selective at an audio frequency of 1200 Hz. Table III below lists values of the bridge capacitors for operation at other frequencies.

RF Amplifiers, Oscillators, and Mixers

The circuit in Fig. 27 is a converter used to convert 10-MHz WWV broadcasts to 1.5 MHz for reception on a standard broadcast-band receiver. The MOS FET IC is used in the dual-gate configuration as a mixer and is triode-

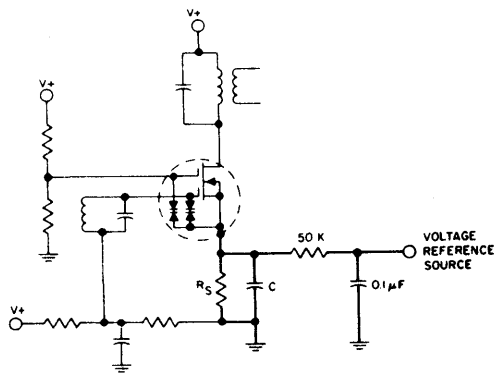


Fig. 20—Typical amplifier using bypassed source resistor as a voltage source.

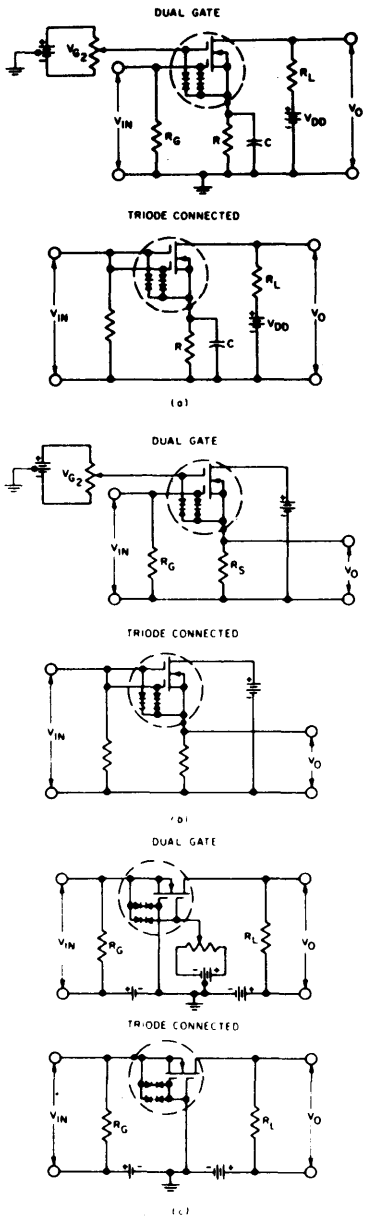


Fig. 21–Three basic single-stage amplifier configurations that use protected dual-gate MOS FET IC's as triodes and tetrodes: (a) common source; (b) common drain; (c) common gate.

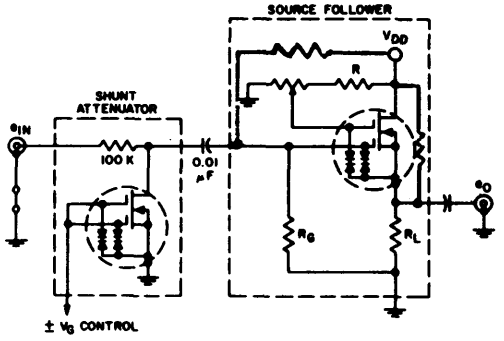


Fig. 22–Shunt-type attenuator controlling input level to source-follower.

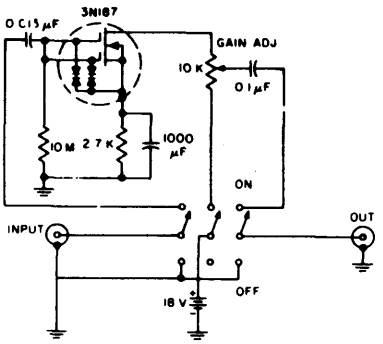


Fig. 23–Protected dual-gate MOS FET IC preamplifier.

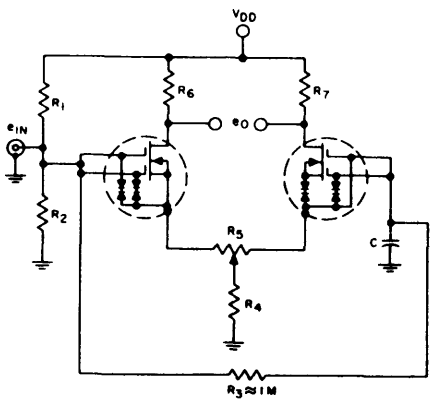


Fig. 24–Triode-connected MOS FET IC's in a simple differential amplifier circuit.

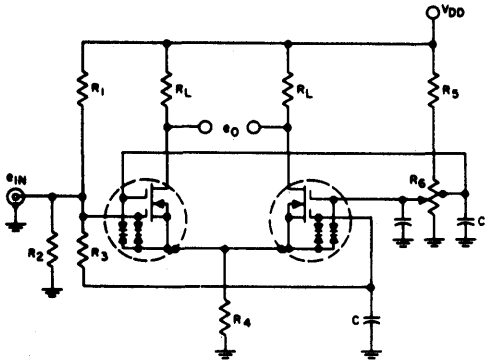


Fig. 25–Protected dual-gate MOS FET IC's in typical differential amplifier circuit using gate 2 for balance control.

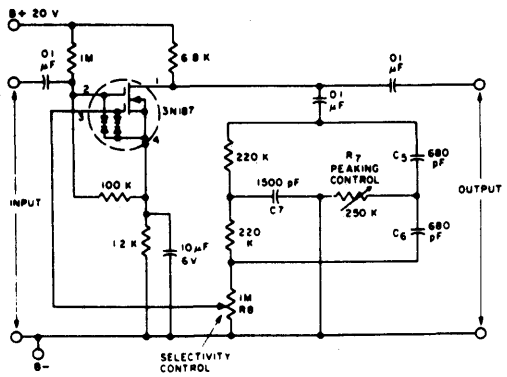


Fig. 26–Selective audio-frequency amplifier.

Table III – Capacitor values for Fig. 26

FREQUENCY (Hz)	C5, C6 (pF)	C7 (pF)
150	5,600	12,000
300	2,700	6,200
600	1,300	3,000
2400	330	750
4800	160	360
9600	82	180

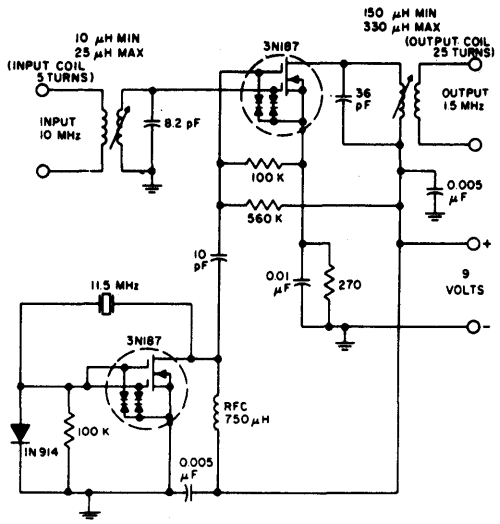


Fig. 27–10 MHz-to-1.5 MHz converter for WWV reception.

connected in a crystal oscillator circuit. MOS FET characteristics are very attractive for use in highly stable oscillator circuits because the inherent reactive components, C_{iss} and C_{oss}, are relatively invariant over a very wide temperature range. Additional types of oscillator circuits in a number of different arrangements are shown in Fig. 28.

It is also feasible to use the MOS FET IC as a keyed oscillator, by utilizing a circuit arrangement shown in Fig. 29. A negative voltage at gate 2 will key the oscillator. Additionally, the level of the oscillator output can be controlled by variation of R_L. It should be understood that any of the oscillator configurations shown above are adaptable to the circuit arrangement in Fig. 29.

A dual-gate-protected MOS FET IC is used in Fig. 30 as a regenerative amplifier/detector. The circuit is basically an amplifier with controlled feedback adjusted to the verge of oscillation, as shown in Fig. 30. Gate 2 provides a convenient means to adjust the amplifier gain to the requisite level. Detection is accomplished in the gate 1 input circuit by the interaction of the diode in parallel with the 100-kilohm resistor and the 270-picofarad capacitor.

A typical circuit that utilizes the MOS FET IC in the pix IF section of a TV receiver is shown in Fig. 31. This circuit utilizes gate 2 for AGC. The reverse AGC bias[7] applied to gate 2 in the circuit of Fig. 31 has the secondary effect of making gate 1 move in a positive direction. Evaluations of the relationship between AGC and crossmodulation show that it is desirable to allow the voltage between gate 1 and the source to move in a positive direction when gate 2 is reverse-biased. Various circuit arrangements have been used

to achieve this action. Reference to a more comprehensive review on crossmodulation as a function of bias is given in the bibliography.[2,3]

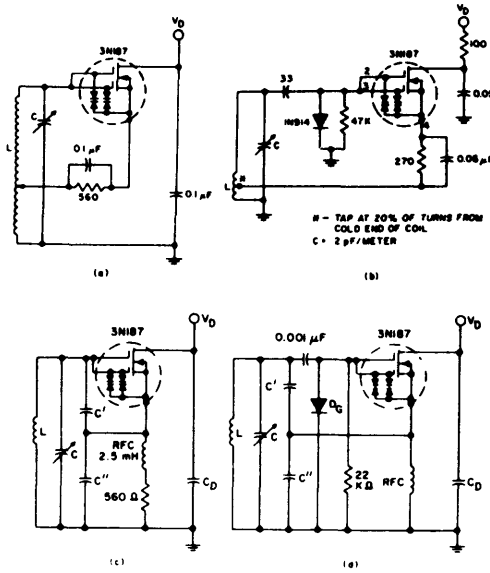


Fig. 28–Oscillator circuits using MOS FET IC's: (a) and (b) Hartley oscillators; (c) and (d) Colpitts oscillators.

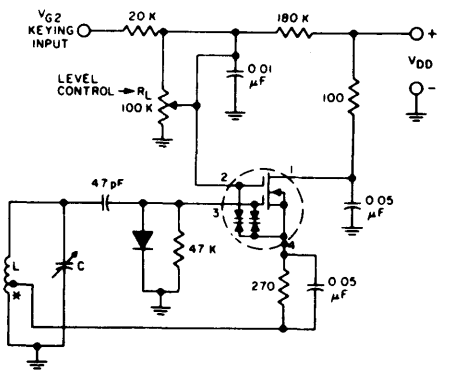


Fig. 29–Gate-keyed oscillator using MOS FET IC.

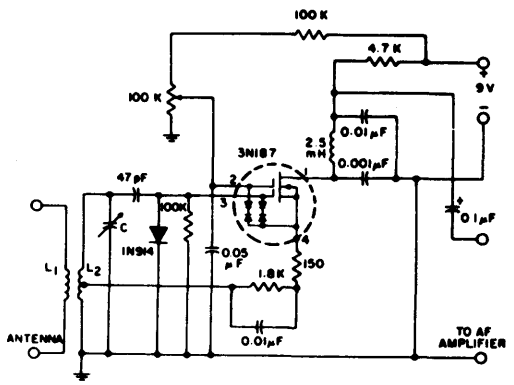


Fig. 30–Protected dual-gate MOS FET IC regenerative receiver.

A typical circuit for an FM tuner is shown in Fig. 32. The biasing arrangement for the rf stage incorporates provisions for AGC. The circuit in Fig. 33 is an rf amplifier designed for 200-MHz operation. The typical power gain for a 3N187 in this circuit is 18 db, with a noise factor of 3.5 dB.

Typical circuits for a TV tuner are shown in Figs. 34(a)-(d). Fig. 34(a) is the rf stage operating at a current level of approximately 10 milliamperes. Gate 1 is about 2 volts above ground potential. When AGC applied to gate 2 is advanced the drain current decreases, with a consequent reduction in voltage drop across the 270-ohm source resistances.[7]

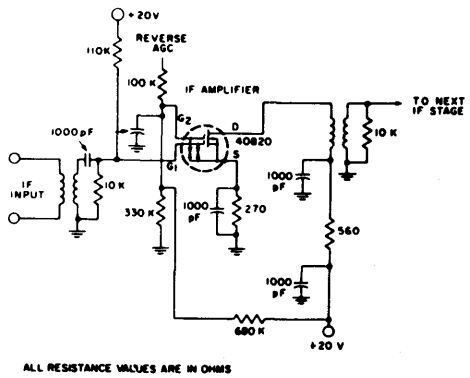
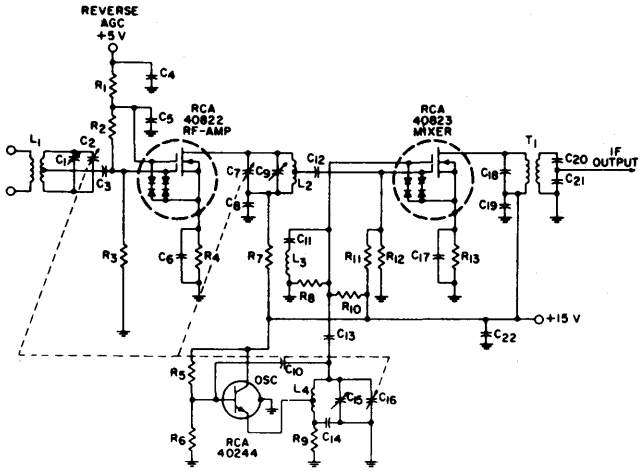
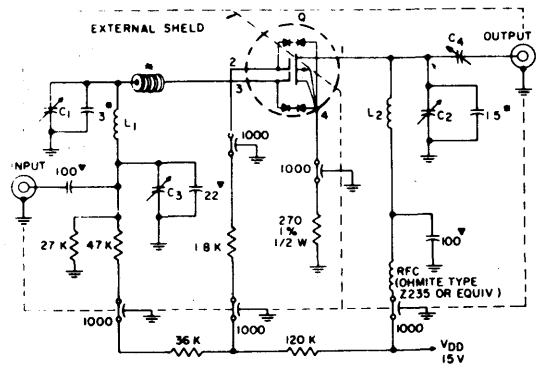


Fig. 31–TV IF amplifier stage utilizing RCA-40820 MOS FET IC.



C1, C9, C15 = Trimmer capacitor, 2 to 14 pF
C2, C7, C16 = Ganged tuning capacitors, each section = 6 to 19.5 pF
C3, C6, C14, C17, C22 = 2000 pF, ceramic
C4, C5 = 1000 pF, ceramic disc
C8, C19 = 0.01 μF, ceramic disc
C10 = 3.3 pF, NPO ceramic
C11 = 270 pF
C12 = 500 pF, ceramic disc
C13 = 3 pF, NPO ceramic
C18 = 68 pF, ceramic
C20 = 50 pF, ceramic
C21 = 1200 pF, ceramic
L1 = antenna coil, 4 turns of No. 18 bare copper wire; inner diameter, 9/32 inch; winding length, 3/8 inch; nominal inductance, 0.86 μH, unloaded Q, 120; tapped approximately 1 1/4 turns from ground end; antenna link approximately 1 turn from ground end
L2 = rf interstage coil, same as L1 antenna link
L3 = rf choke, 1 μH
L4 = oscillator coil; 3 1/4 turns of No. 18 bare copper wire; inner diameter, 9/32 inch; winding length, 5/16 inch; nominal inductance, 0.062 μH, unloaded Q, 120; tapped approximately 1 turn from low end
R1, R10 = 0.56 megohm, 0.5 watt
R2 = 0.75 megohm, 0.5 watt
R3 = 0.27 megohm, 0.5 watt
R4, R13 = 270 ohms, 0.5 watt
R5 = 22000 ohms, 0.5 watt
R6 = 56000 ohms, 0.5 watt
R7 = 330 ohms, 0.5 watt
R8, R12 = 0.1 megohm, 0.5 watt
R9 = 4700 ohms, 0.5 watt
R11 = 1.6 megohms, 0.5 watt
T1 = first if (10.7 MHz) transformer; double-tuned with 90 per cent of critical coupling; primary: 15 turns of No. 32 enamel wire, space wound at 60 turns per inch on 0.25-by-0.5-inch slug; secondary: 18 turns of No. 36 enamel wire, close wound on 0.25-by-0.25 inch slug; both coils wound on 9/32-inch coil form.

Fig. 32–FM tuner using RCA-40822 and RCA-40823 MOS FET IC's for the rf amplifier and mixer stages.



#Ferrite bead (4); Pyroterric Co. "Carbonl J" Q = 3N187
0.09 in. OD; 0.03 in. ID; 0.063 in. thickness. ▼ Disc ceramic
All resistors in ohms • Tubular ceramic
All capacitors in pF
C1 = 1.8-8.7 pF variable air capacitor: E.F. Johnson Type 160-104, or equivalent.
C2 = 1.5-5 pF variable air capacitor: E.F. Johnson Type 160-102, or equivalent.
C3 = 1-10 pF piston-type variable air capacitor: JFD Type VAM-010; Johanson Type 4335, or equivalent
C4 = 0.8-4.5 pF piston type variable air capacitor: Erie 560-013 or equivalent.
L1 = 4 turns silver-plated 0.02-in. thick, 0.075-0.085-in. wide, copper ribbon, internal diameter of winding = 0.25 in., winding length approx. 0.08 in.
L2 = 4½ turns silver-plated 0.02-in. thick, 0.085-0.095-in. wide, 5/16 in. ID. Coil = .90 in. long.

Fig. 33–200-MHz amplifier using the RCA-3N187 MOS FET IC.

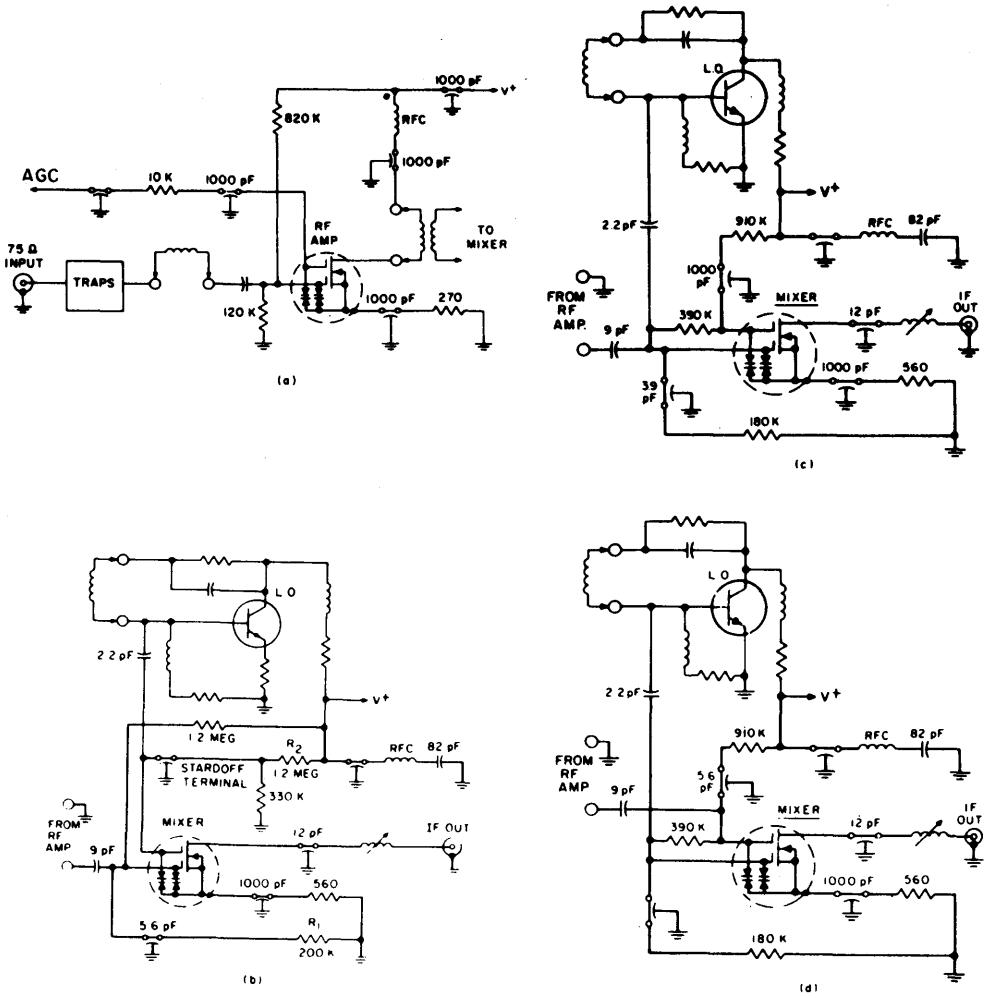


Fig. 34—Typical circuits using protected dual-gate MOS FET IC's in a TV tuner for (a) rf stage, (b) mixer with rf on gate 1, oscillator on gate 2; (c) mixer with both rf and oscillator on gates 1 and 2; (d) mixer with rf on gate 2 and oscillator on gate 1.

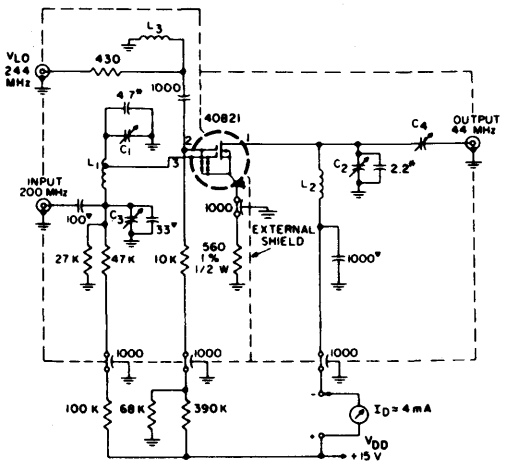
Because the voltage on gate 1 is fixed, the effect of applying AGC is to make the gate-to-source voltage drift in a positive direction as a negative gate 2 (AGC) voltage is applied. In these cases, as in the earlier IF system shown in Fig. 31, this circuit arrangement optimizes tuner performance for crossmodulation.[2]

The rf stage in Fig. 34(a) can work into any of the mixer circuits shown in Figs. 34(b), (c), and (d).

Fig. 34(b) is a mixer circuit arrangement with oscillator injection into gate 2 and the rf signal applied to gate 1. Fig. 34(c) utilizes gate 1 and gate 2 as the input elements for both rf signal and oscillator. Fig. 34(d) shows the rf signal applied to gate 2 and oscillator injection on gate 1.

Each of the above circuit arrangements has its own desirable characteristics, and the subject of mixer performance deserves a much more detailed discussion than can be accommodated here. In this context it is intended to demonstrate feasibility in terms of circuit arrangements.

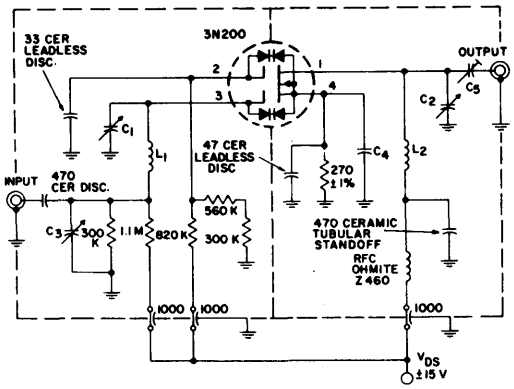
A mixer circuit with component values used in the laboratory for measuring conversion power gain from 200 to 44 MHz is shown in Fig. 35.[8]



▼ Disc. ceramic.
* Tubular ceramic.
All resistors in ohms
All capacitors in pF
C1, C2 = 1.5-5 pF variable air capacitor: E.F. Johnson Type 160-102 or equivalent.
C3 = 1-10 pF piston-type variable air capacitor: JFD Type VAM-010, Johanson Type 4335, or equivalent.
C4 = 0.9-7 pF compression-type capacitor: ARCO 400 or equivalent
L1 = 5 turns silver-plated 0.02" thick, 0.07"-0.08" wide copper ribbon. Internal diameter of winding = 0.25"; winding length approx. 0.65". Tapped at 1-1/2 turns from C1 end of winding.
L2 = Ohmite Z-235 RF choke or equivalent.
L3 = J.W. Miller Co. #4580 0.1 μH RF choke or equivalent.
NOTE: If 50Ω meter is used in place of sweep detector, a low pass filter must be provided to eliminate local oscillator voltage from load.

Fig. 35—Mixer circuit for 200 MHz-to-44 MHz conversion, using the RCA-40821 MOS FET IC.

Protected dual-gate MOS FET's have been used in applications operating at frequencies up to 500 MHz. They are useful in such uhf applications as rf amplifiers and mixer circuits. For example, the RCA-3N200 has the capability to provide a typical rf power gain of 12.5 dB with 4.5-dB noise factor at 400 MHz in a common-source configuration without the need for neutralization. A circuit with this capability is shown in Fig. 36.



All resistances in ohms
All capacitances in pF
C1, C2 = 1.3-5.4 pF variable air capacitor: Hammerland Mac 5 type or equivalent
C3 = 1.9-13.8 pF variable air capacitor: Hammerland Mac 15 type or equivalent
C4 = Approx. 300 pF - capacitance formed between socket cover & chassis
C5 = 0.8-4.5 pF piston type variable air capacitor: Erie 560-013 or equivalent
L1, L2 = inductance to tune circuit

Fig. 36—Using the RCA-3N200 MOS FET IC in a 400-MHz amplifier.

CONCLUSIONS

The preceding discussions outlined numerous practical applications that utilized the unique technical features of the RCA protected dual-gate MOS FET IC. A summary of these technical features includes:

1. Wide dynamic range – MOS FET IC's will handle both positive and negative signal excursions.
2. Crossmodulation and spurious response performance is inherently better than with other active devices such as bipolars and single-gate FET's.
3. The very low gate-leakage permits AGC circuitry with virtually no power requirements.

BIBLIOGRAPHY

1 S.R. Hofstein and F.P. Heiman, "The Silicon Insulated Gate Field-Effect Transistor", Proc. I.EEE, Vol. 51, No. 9, pp. 1190-1202, September, 1963.

2 E.F. McKeon "Crossmodulation Effects in Single Gate and Dual Gate MOS Field Effect Transistors" RCA Application Note AN-3435.

3 S. Reich and L.S. Baar, "A Comparison of Solid-State and Electron Tube Devices For TV-Receiver RF and IF Stages." IEEE Transactions on Broadcast and TV Receivers, Vol. BTR-13, pag. 41, April 1967.

4 J.R. Burns, "High Frequency Characteristics of Two Insulated Gate Field Effect Transistor" RCA Review, Vol. XXVIII No. 3, Sept. 1967, pp. 385-417.

5 3N187 Data Sheet, RCA File #436.

6 3N200 Data Sheet, RCA File #437.

7 S. Reich, "MOS FET Biasing Techniques," EEE, Sept. 1970.

8 L.S. Baar, "RF Applications of the Dual Gate MOS FET Up to 500 MHz" RCA Application Note AN-4431.

4. Two input control elements make the device adaptable for mixers, remote-control gain circuits, coincidence gate circuits, etc. The device can also function as a triode-equivalent when the two gates are connected to a single terminal.
5. An exceptionally high transconductance.
6. Negative temperature coefficient for drain current, so that thermal runaway is virtually impossible.
7. Extremely low feedback capacity, typically 0.02 picofarad; this means very low oscillator feedthrough from the mixer stage back to the antenna.
8. The low feedback capacity enables the dual-gate MOS FET IC to provide good rf power gain in common-source amplifiers without the need for neutralization.
9. In addition to the above features, the new MOS FET IC provides protection against static electricity discharges encountered during handling and/or in circuit applications. This protection was achieved with insignificant compromises in overall device performance.