

Circuit provides more accurate multiplication

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Common analog multiplying devices employ methods using transistor parameters. Precise versions of these devices use the logarithm method of multiplication. This method involves the addition of logarithms and an exponential conversion (Reference 1). Using these methods, you can achieve a minimal error of $\pm 0.1\%$. This Design Idea reduces the error, employs readily available standard components, and maintains the correct voltage scale.

The structure squares the sum and the difference of both components of the desired multiplication. The difference of these squared values yields the result of the multiplication. You can scale the desired multiplication of a and b using the identity of $4ab=(a+b)^2-(a-b)^2$.

In a conceptual diagram, blocks 1 and 2 represent the input part of the device (Figure 1). They comprise identical precise rectifiers. You implement these rectifiers with amplifiers A_1 , A_2 , A_3 , and A_4 (Figure 2). They provide the addition and the subtraction of input voltages V_A and V_B . The rectifiers create the output voltages $k(V_A+V_B)$, $k(V_A-V_B)$, which have only positive polarity. You connect these outputs to a two-channel ADC, Block 3, and then to two identical DACs: DAC₁ (Block 4) and DAC₂ (Block 5).

The ADC converts $k(V_A+V_B)$ and $k(V_A-V_B)$ to proportional codes N_1 and N_2 . The ADC must handle the conversion over the full range of the absolute sum $|k(V_A+V_B)|$. The reference

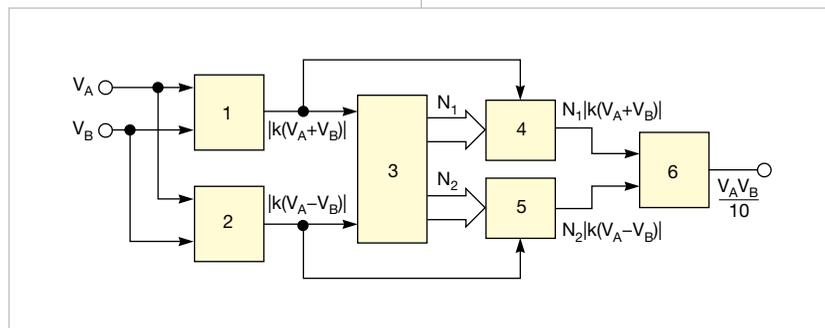


Figure 1 Perform a multiplication of two values, V_A and V_B , by using ADCs, DACs, and amplifiers to do the mathematics of an equivalent expression.

TABLE 1 RESULTS OF FOUR QUADRANTS

V_A (V)	V_B (V)	$k(V_A+V_B)$ (V)	$k(V_A-V_B)$ (V)	N_1	N_2	V_5 (V)	V_6 (V)	V_5-V_6 (V)
5	3	4	1	0.4	0.1	-1.6	-0.1	1.5
5	-3	1	4	0.1	0.4	-0.1	-1.6	-1.5
-5	3	1	4	0.1	0.4	-0.1	-1.6	-1.5
-5	-3	4	1	0.4	0.1	-1.6	-0.1	1.5

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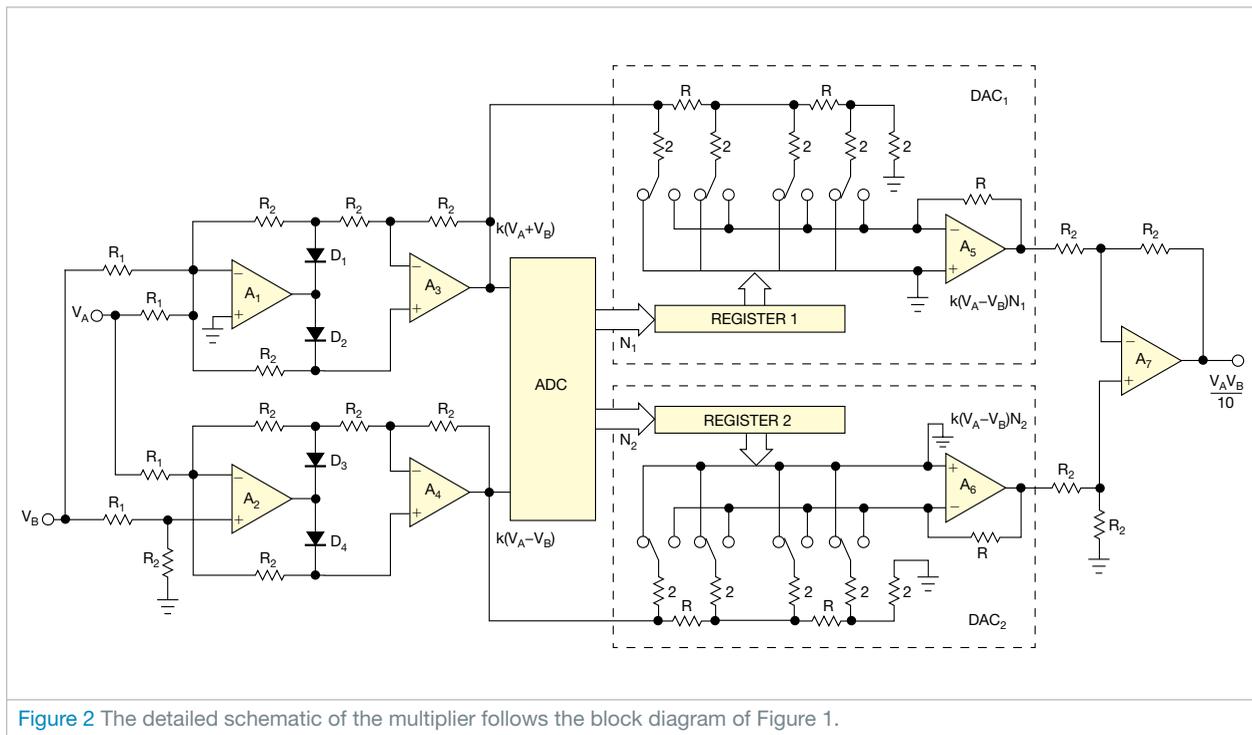
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voltage of the ADC should be equal to the maximum expected value of $|k(V_A+V_B)|$. Codes N_1 and N_2 translate to Register 1 of DAC₁ and Register 2 of DAC₂, respectively (Reference 2). These codes establish the values on the R-2R dividers of each DAC. The output voltages of blocks 4 and 5, comprising $N_1|k(V_A+V_B)|$ and $N_2|k(V_A-V_B)|$, pass through operational amplifier A_7 in Block 6. You configure the op amp with a differential input, which takes the difference between the inputs and creates the multiplication result on the output. For example, if both voltages V_A and V_B have a range of $\pm 10V$ and the input range of the ADC is 0 to 10V, then coefficient $k=R_2/R_1=0.5$. The full sum of each part should be $\pm 10V$. Table 1 provides the results for all four quadrants of these conditions.

The systematic error of the multiplication is the sum of the discrete errors



of the ADC and both DACs. This error depends on the resolutions of these devices. Choosing an ADC and DACs with greater resolutions will further reduce the overall error.**EDN**

REFERENCES

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