Fast-settling low-pass filter circuit

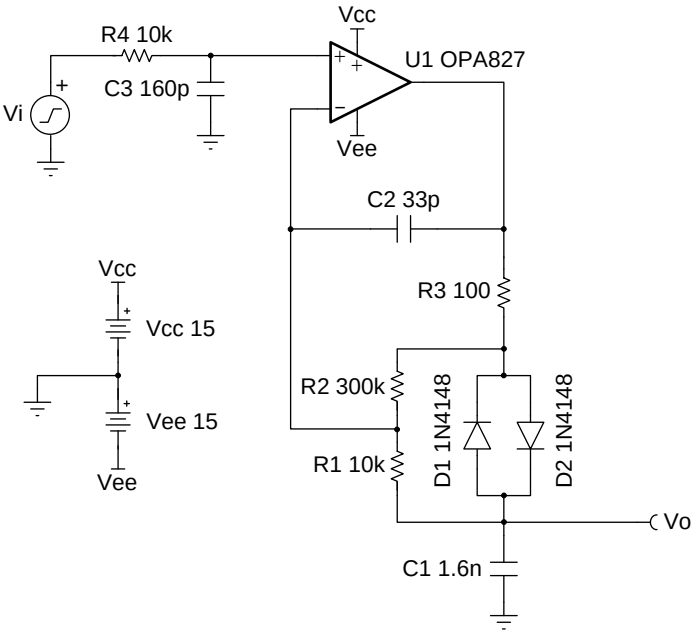
Design Goals

Input		Output		Supply	
V_{iMin}	V_{iMax}	V_{oMin}	V_{oMax}	V_{cc}	V_{ee}
–12V	12V	–12V	12V	15V	–15V

Cutoff Frequency (f_c)	Diode Threshold Voltage (V_t)
10kHz	20mV

Design Description

This low-pass filter topology offers a significant improvement in settling time over the conventional single-pole RC filter. This is achieved through the use of diodes D_1 and D_2, that allow the filter capacitor to charge and discharge much faster when there is a large enough difference between the input and output voltages.



Design Notes

1. Observe the common-mode input limitations of the op amp.
2. Keeping C_1 small will ensure the op amp does not struggle to drive the capacitive load.
3. For the fastest settling time, use fast switching diodes.
4. The selected op amp should have sufficient output drive capability to charge C_1. R_3 limits the maximum charge current.

Design Steps

1. Select standard values for R_1 and C_1 based on f_C = 10kHz.

   $R_1 = 10k\Omega$

   $C_1 = \frac{1}{2\pi \times f_C \times R_1} = \frac{1}{2\pi \times 10kHz \times 10k\Omega} = 1.6nF$

2. Set the diode threshold voltage (V_t). This threshold is the minimum difference in voltage between the input and output that will result in diode conduction (fast capacitor charging and discharging).

   $V_t = \frac{V_f}{1+\frac{R_2}{R_1}} \approx \frac{0.6V}{1+\frac{R_2}{R_1}} = 20mV$

   $R_2 = (\frac{0.6V}{20mV} - 1) \times R_1 = 290k\Omega \approx 300k\Omega$ (standard 5% value)

3. Select components for noise pre-filtering.

   $f_{c2} = 10 \times f_c = 100kHz$

   $f_{c2} = \frac{1}{2\pi \times R_4 \times C_3}$

   Select $R_4 = R_1 = 10k\Omega$

   $C_3 = \frac{C_1}{10} = 160pF$

4. Add compensation components to stabilize U_1. R_3 limits the charge current into C_1 and also serves to isolate the capacitance from the op amp output when the diodes are conducting. Larger values will improve stability but increase C_1 charge time.

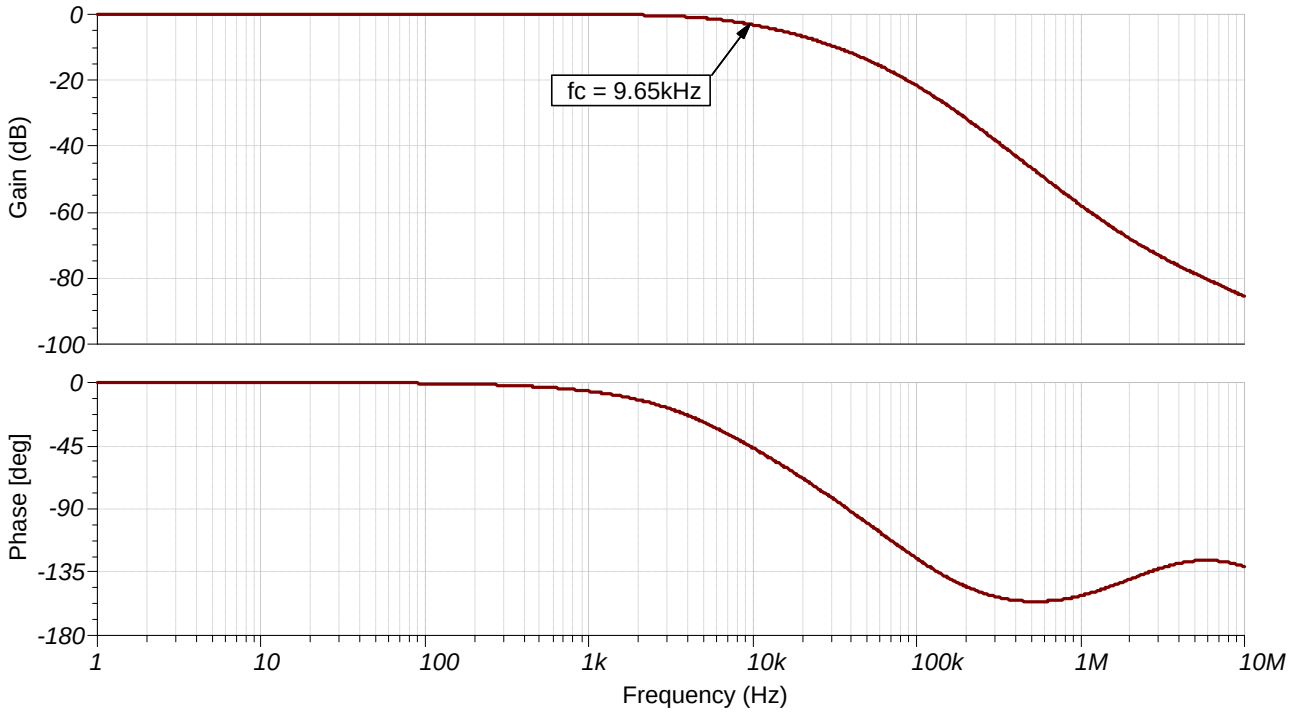
   Select $R_3 = 100\Omega$

5. C_2 provides local high frequency feedback to counteract the interaction between the input capacitance with the parallel combination of R_1 and R_2. To prevent interaction with C_1, select C_2 as the following shows:

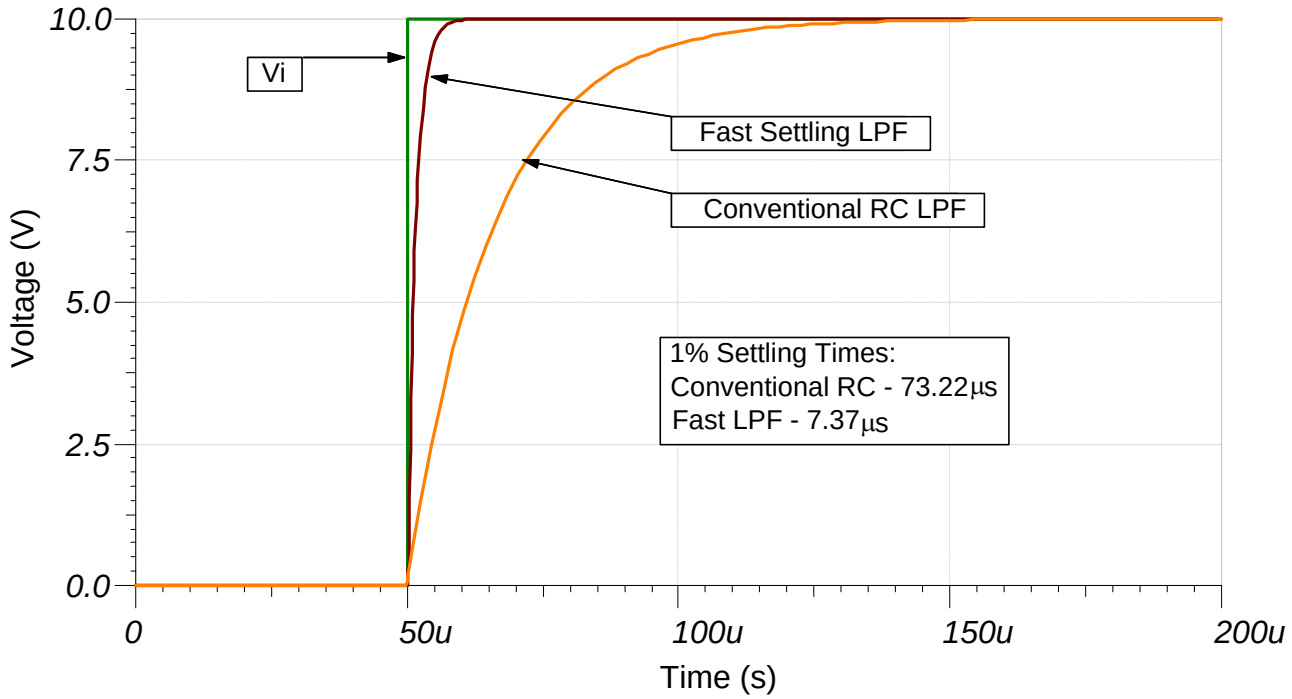
   Select $C_2 = \frac{C_1}{50} = 32pF \approx 33pF$ (standard value)

Design Simulations

AC Simulation Results



Transient Simulation Results



Design References

See Analog Engineer's Circuit Cookbooks for TI's comprehensive circuit library.

See TINA-TI™ circuit simulation file, SBOMAU1.

For more information on many op amp topics including common-mode range, output swing, bandwidth, and how to drive an ADC, see TI Precision Labs.

Design Featured Op Amp

OPA827	
V_{ss}	8V to 36V
V_{inCM}	V_{ee}+3V to V_{cc}–3V
V_{out}	V_{ee}+3V to V_{cc}–3V
V_{os}	75µV
I_q	4.8mA
I_b	3pA
UGBW	22MHz
SR	28V/µs
#Channels	1
http://www.ti.com/product/opa827	

Design Alternate Op Amp

TLC072	
V_{ss}	4.5V to 16V
V_{inCM}	V_{ee}+0.5V to V_{cc}–0.8V
V_{out}	V_{ee}+350mV to V_{cc}–1V
V_{os}	390µV
I_q	2.1mA/Ch
I_b	1.5pA
UGBW	10MHz
SR	16V/µs
#Channels	1,2,4
http://www.ti.com/product/tlc072	