The Liniac

A new linear inverting and amplifying circuit and some other applications of low-level Darlington transistors

by J. L. Linsley Hood

One of the most interesting of recent developments in the discrete semiconductor components field has been the use of integrated circuit techniques to provide small-signal Darlington-connected transistors of the general form shown in Fig. 1(a). A suggested symbol is given in Fig. 1(b), and this is used in the remainder of this article.

While it is practicable to construct Darlington pairs from separate transistors if the collector current of the second transistor is fairly large, at the sort of current levels typically employed in small signal circuitry it is much more difficult. If the second transistor has, say, a current gain of 400 and a collector current of 0·5 mA, the collector current of the first device must be less than 1·25 μA, and at this order of collector current the current gain of most normal discrete small-signal transistors is very low, and their other characteristics are also impaired.

When, however, a monolithic Darlington transistor is made, the junction areas and doping levels of the input transistor are adjusted so that it will function effectively at a very low collector current. Also, because of the very low collector-to-input base capacitance, it is possible to obtain good performance at moderately high frequencies, even with high dynamic impedance collector loads, which give high stage gain values.

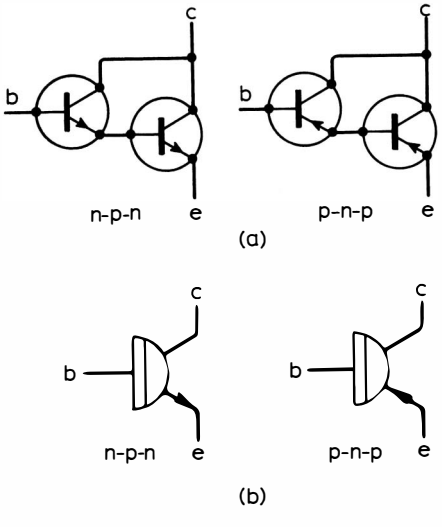


Fig. 1. (a) Darlington transistor arrangements; (b) suggested symbol for monolithic Darlington devices.

Ideally, a low-level amplifier element should have a high input impedance, a relatively low output impedance, a high gain, a low noise level, should be linear, should be simple and tolerant in its power supply requirements. The normal (bipolar) junction transistor does not meet the input and output impedance requirements at all well, and in addition is intrinsically non-linear as a voltage amplifying element, so that it is almost essential to arrange stages in cascade with substantial amounts of overall negative feedback to remedy these defects. However, on consideration it is apparent that the non-linearity of the bipolar transistor is an input characteristic effect, and for any given base-emitter circuit impedance is directly related to the magnitude of the input signal voltage. Within limits, the output signal swing is unimportant in this respect. It follows from this that for any given output signal level, the higher the gain of the stage the better its linearity will be. The monolithic Darlington transistor offers a satisfactorily high input impedance with a very high value of current gain, and if an arrangement can be found in which this can be induced to give a high voltage gain the major circuit requirements will have been met. Moreover, such a stage will be phase inverting which is very convenient for a number of applications, whereas the conventional transistor feedback pairs of Fig. 2 are non-inverting systems.

Methods of obtaining high stage gain

Several techniques are available for increasing the stage gain of a conventional transistor amplifier. However, some of these are unhelpful in preserving the linearity of the system, and the principal remaining technique is to employ a collector load which has a dynamic impedance substantially larger than its d.c. resistance. This could be a "bootstrapped" load resistor, an "active" (i.e. signal dependent) load, or a constant-current source. Of these arrangements the third is by far the most straightforward and free from side-effects, and such a constant-current load can be provided by the use of a conventional junction field-effect transistor, for which the circuit required, as shown in Fig. 3, is simplicity itself. The characteristics of this arrangement are shown in Fig. 4 for various values of the source resistor R_1.

Since the dynamic resistance of such a system is, effectively proportional to the reciprocal of the slope of the drain-current/drain-voltage graph (i.e., the flatter the higher) it can be seen that there are conditions when this dynamic impedance is very high, and it could then be employed as the load in the collector circuit of a transistor amplifier stage. This would give a very high

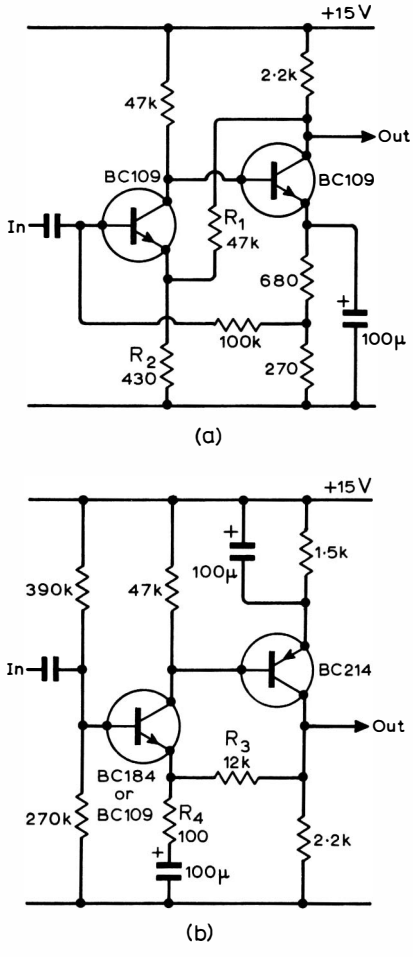


Fig. 2. Feedback stabilized non-phase-inverting transistor pairs. (a) n-p-n/n-p-n feedback pair. Gain depends on R_1, R_2 (as shown $M \approx 100$). Input impedance ≈ 68 kΩ. Open loop gain ≈ 2000. (b) n-p-n/p-n-p pair. Gain depends on R_3, R_4 (as shown $M \approx 100$). Input impedance ≈ 50 kΩ. Open loop gain ≈ 2000.

stage gain while still allowing a reasonable value for the collector current, and a convenient range of voltage drop values across the load. Moreover, by the suitable choice of f.e.t. or source resistor the collector current of the amplifying transistor can be precisely defined, which is frequently an advantage.

Circuit conditions for high stage gain

The stage gain of a simple single-stage transistor amplifier is given by the formula.

$$M = \frac{1}{h_{re} - \frac{h_{ie}}{Z_L}\left(\frac{1+h_{oe}.Z_L}{h_{fe}}\right)}$$

If the terms $(h_{ie}.h_{oe} - h_{fe}.h_{re})$ are written as Δh_e, the so-called "h determinant" for the common emitter configuration, this equation simplifies to

$$M = \frac{h_{fe}.Z_L}{\Delta h_e.Z_L + h_{ie}}$$

and if Δh_e is sufficiently small, as is mostly the case, this approximates to

$$M \approx \frac{h_{fe}.Z_L}{h_{ie}}$$

If the dynamic value of Z_L is large, and the input impedance of the amplifier transistor is small the stage gain can be very high. (However, h_{ie} depends on the collector current of the transistor, and increases as this is reduced. For this reason, high gains normally require both a certain minimum of collector current and also a drive impedance which is small in relation to h_{ie}.)

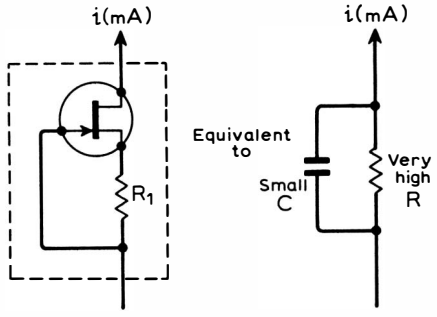


Fig. 3. Constant current load using f.e.t.— i depends on f.e.t. and value of R_1. Dynamic impedance in range 200 kΩ–2 MΩ.

As will be seen from Fig. 4, an f.e.t. will act as a high dynamic impedance constant-current source even when the source resistance R_1 has zero value, provided that the source-drain voltage exceeds what is known as the "pinch-off" voltage, which is typically two or three volts. The current which will flow in this condition (zero source-gate bias) is known as the I_{DSS} and will depend on the device. For f.e.ts such as the 2N4302 and the 2N5457 this will be in the range 1–3 mA—a convenient value of collector current at which to operate a typical small signal Darlington amplifier stage. When such a transistor amplifier is employed with an f.e.t. collector load it is found that stage gains of the order of 2500 to 5000 can be obtained, even with source impedances of the order of 100 kΩ or more.

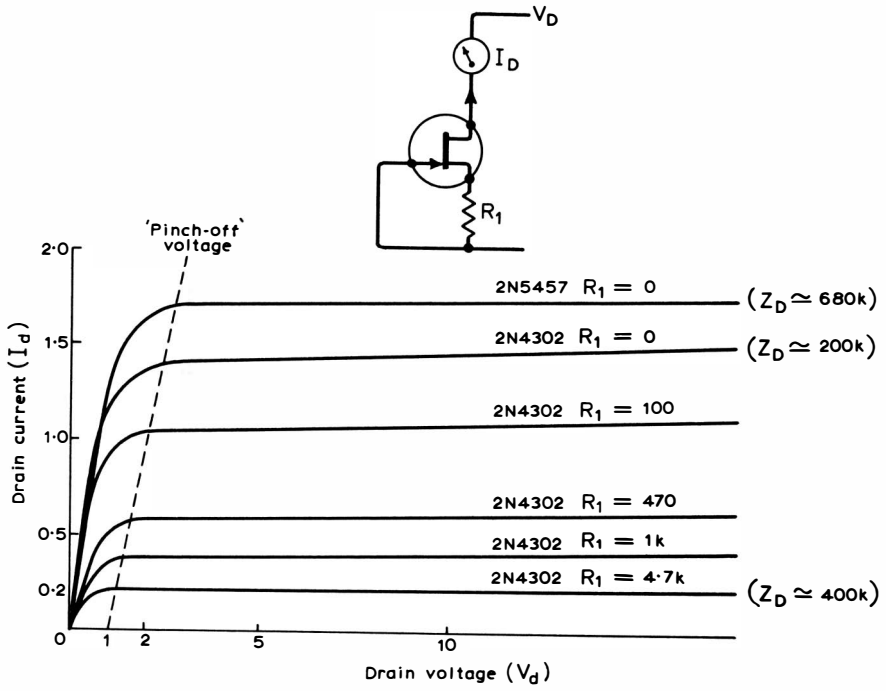


Fig. 4. Drain current characteristics for sharp cut-off f.e.ts.

It will be appreciated that an amplifier stage of this type using a high dynamic impedance collector load will have an output impedance which is so high that the shunting effect of almost any external load would lead to a serious reduction in gain. To complete the practical circuit, therefore, an output emitter follower is required, and this can with advantage be a further monolithic Darlington transistor, although in practice a normal high-grain small signal transistor may be nearly as good and somewhat cheaper.

The final form of the proposed high gain circuit combination is shown in Fig. 5(a), and for convenience as a "shorthand" form in Fig. 5(b). This circuit arrangement has been found to be very versatile as a relatively low-frequency amplifier stage, and to possess a number of useful qualities as a phase-inverting circuit element, and the name "liniac" (linear inverting amplifying circuit) is suggested for this configuration.

Liniac circuit characteristics

General considerations. In its simplest form, the liniac consists of a bipolar transistor connected as a grounded-emitter amplifier, an f.e.t. used as a constant current load, and an output emitter follower. If the output circuit impedance is fairly high, say 10 kΩ or greater, this can be a normal small-signal transistor such as the BC109 or BC184. Also, if a source resistor is used with the f.e.t. of a value sufficient to reduce the load current to some 10–50 μA (at which level the dynamic impedance is extremely high)

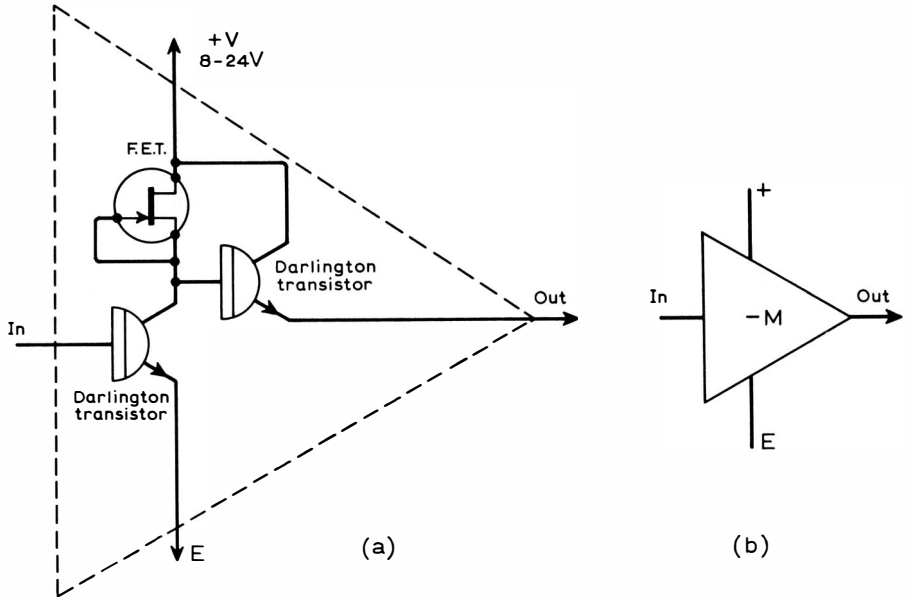


Fig. 5. (a) Basic liniac configuration; (b) symbol proposed for liniac.

and if a very high input impedance is not required, a simple bipolar transistor of similar type can also be used as the amplifier stage. This is the system which is to be preferred if the lowest possible noise level is required, and is still capable of very high stage gains if the drive impedance is fairly low. But, for most applications, a monolithic Darlington device is preferred in this position since this has a lower collector/base feedback capacitance and therefore gives a better open-loop h.f. response.

The liniac arrangement can be made with devices of complementary symmetry, with appropriate adjustments to supply polarity, and since the f.e.t. is used as a two-terminal unit either n-channel or p-channel devices can be employed provided that they have suitable I_{DSS} and pinch-off voltage values. A suitable arrangement using a single very low noise p–n–p input transistor is shown in Fig. 6.

Stage gain. Because of the low emitter-circuit impedance of the amplifier transistor when a Darlington device is used in this position, and because of the high dynamic impedance of the collector load, the gain of the circuit is very high—typically of the order of several thousands—even when fed from a high source impedance, and is limited, at low frequencies, mainly by the output impedance (Z_{oe}) of the amplifier transistor, which is effectively in parallel with the collector load. At higher frequencies, the effect of the collector shunt and Miller capacitances causes the gain to fall at −6 dB/octave. Typical gain/frequency characteristics are shown in Fig. 7.

Distortion characteristics. For the reasons mentioned above, this configuration will be expected to possess a significantly lower order of non-linearity than the conventional bipolar transistor amplifier using a normal resistive load. In the event, the non-linearity is reduced by the same factor by which the gain of the stage is increased in comparison with the normal bipolar transistor operated at the same collector current. This is typically 10–15 times, which is a valuable feature in audio amplification circuitry. The output-voltage/total-harmonic distortion characteristics are shown in Fig. 8. Since in normal circuit applications overall negative feedback will be employed, and this will reduce the non-linearity even further, a stage with a gain of 50× can be built with less than 0·005% t.h.d. at 1 kHz at 1 V r.m.s. output.

Noise levels. The noise characteristics of the circuit, at gain levels in excess of some 20× (assuming some externally applied negative feedback) depend mainly upon the characteristics of the device used as the amplifier transistor, and on the relationship between the collector current and the input circuit impedance. The best available low-noise small-signal transistors give noise figures which are about twice as good as the equivalent monolithic Darlington connected devices. For this reason, when the liniac circuit is to be used under conditions where the noise level is of importance, such as in the input stage of a high-gain amplifier, it may be preferred to use the simple bipolar type, but in this case a lower input circuit impedance is essential.

In common with other transistor types the noise level at the output is reduced as the collector-emitter potential is reduced. For example, reducing the collector voltage from 8 V to 2·5 V reduces the broad band noise by about a factor of two, but also, of course, reduces the available output voltage swing. This technique should, therefore, be used with discretion.

At stage gains less than 20, the noise contribution due to the f.e.t. may also become important, since the circuit can equally well be visualized as an f.e.t. amplifier with a bipolar constant current load, and if it is intended to use the stage with an output voltage of less than 100 mV, a low-noise f.e.t. should be used. The use of an unbypassed source resistor in the f.e.t. circuit will also reduce its noise contribution.

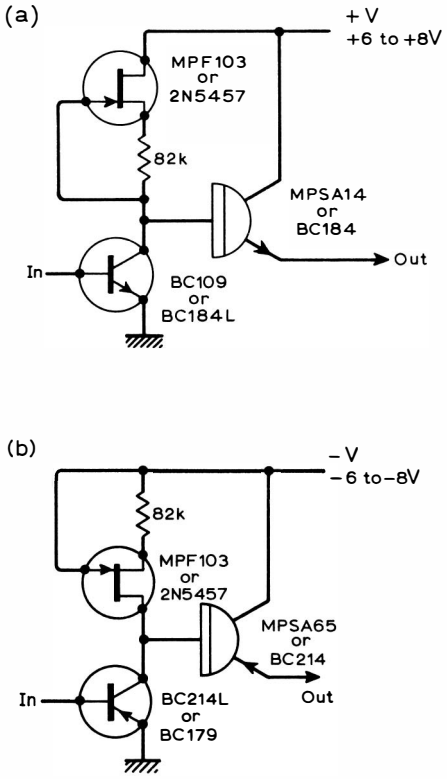


Fig. 6. Very low noise modified liniac arrangements. Gain 2000–4000.

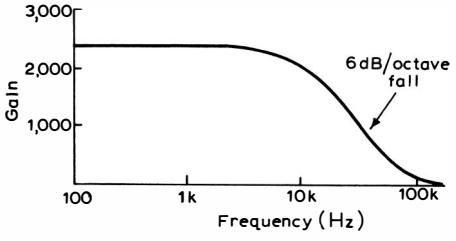


Fig. 7. Typical open-loop gain/frequency characteristics of liniac using Darlington input stage (as circuit of Fig. 9(a)).

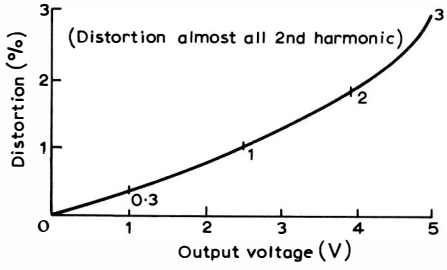


Fig. 8. Output signal voltage/distortion characteristics of liniac stage without negative feedback—Fig. 9(a). $V_c(Tr_1) = 8$ V.

Supply-line ripple rejection. One of the more desirable qualities of small-signal amplifying stages is that they should not be affected to any large extent by ripple, voltage fluctuations or signal feedback from the h.t. supply line. This helps to eliminate hum, instability, and unexpected sources of distortion or cross-talk. Since the collector load of the transistor amplifier stage is a good constant-current source, and in typical circuit applications the input bias is not derived from the h.t. line the output signal is largely isolated from supply fluctuations. This advantage is diminished somewhat by the fact that the amplifier transistor has also a high dynamic impedance, but nevertheless the supply line rejection characteristics—assisted by externally applied negative feedback—are much better than those of the normal bipolar amplifier circuit.

Supply and output voltages. In typical liniac circuit applications, such as those shown in Fig. 9 *et seq*, closed-loop d.c. negative feedback is employed to stabilize the working voltage levels. This allows precise control of the collector potential of the first transistor stage, and thereby determines the potential drop across the f.e.t. collector load. Since it is undesirable that this should operate on the curved portion of its characteristic (*cf.* Fig. 4) the h.t. voltage level should be chosen so that there is at least 3 V across the f.e.t. at the peaks of the signal swing. Since the amplifier transistor should also be biased so that there is a minimum of some 2 V across it at the bottom end of the signal swing, the appropriate voltage levels may be determined simply if the output voltage swing is specified.

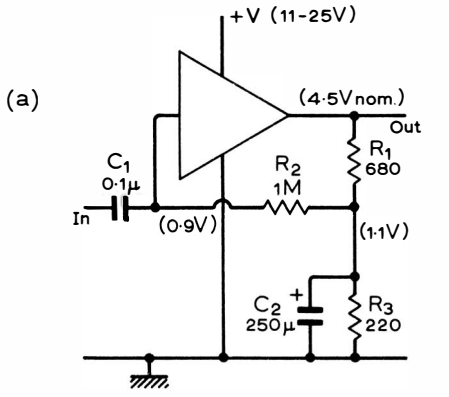
For example, if it is desired that the output should be 2 V r.m.s., which is 2·83 V peak, the collector voltage of the amplifier transistor should be at least 2 plus 2·83 V—say 5 V. Similarly the h.t. supply should be 3 V plus 2·83 V above this level—say 11 V. Since the forward base-to-emitter voltage drop of the Darlington transistor is some 0·9 V, the output level corresponding to the desired first transistor collector potential will be 4·1 V, assuming a Darlington device is used as the output emitter follower. If a simple transistor is employed the desired output voltage level will be 4·5 V.

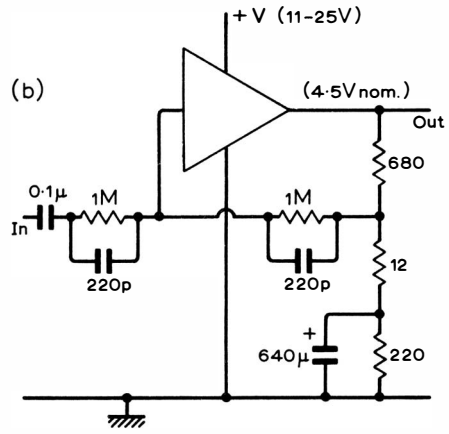
The Darlington transistor used in the first stage will conduct when the base emitter potential exceeds 0·8–0·9 V R_1 and R_3 are chosen to give this—Fig. 9(a). Because of phase shift introduced by the interaction of C_1 and C_2 in this particular circuit, there will be a "hump" in the gain curve at about 10 Hz (with the capacitor values quoted) if the circuit is driven from a low-impedance source. If this is inconvenient it can be removed by a suitable input time constant

high-pass *CR* circuit.

In Fig. 9(b) the circuit has been elaborated to incorporate loop negative a.c. feedback to give a very-low-distortion amplifier with a gain of 50 and a wide bandwidth—10 Hz to 80 kHz at 3 dB—with the same d.c. levels and an input imepdance of 1 MΩ.

A simpler wide bandwidth arrangement using a lower input impedance is shown in Fig. 9(c). In this and the previous circuit a "virtual earth" feedback arrangement is employed. It should be remembered that in such cases the gain is dependent on the input circuit impedance as well, and an allowance should be made for this in the design considerations. There are obviously a large number of permutations of these basic circuits, but some specific applications are shown below, in which facility for output to input loop negative feedback is exploited.





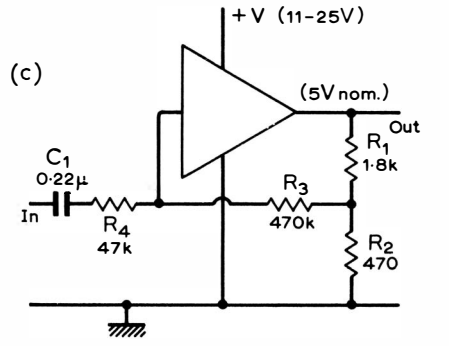


Fig. 9. (a) Typical high-gain liniac amplifier stage V_{out} = 2 V r.m.s. (max.). Gain ≈ 2500. Input impedance ≈ 100 kΩ. (b) High input impedance liniac arrangement. V_{out} = 2 V r.m.s. (max.). Gain ≈ 50. Input impedance ≈ 1 MΩ (and 120 pF). Bandwidth (−3 dB) 10 Hz–80 kHz. (c) Low distortion liniac amplifier stage. Gain ≈ 50. T.H.D.< 0·01% at 2 V r.m.s. output (1 kHz).

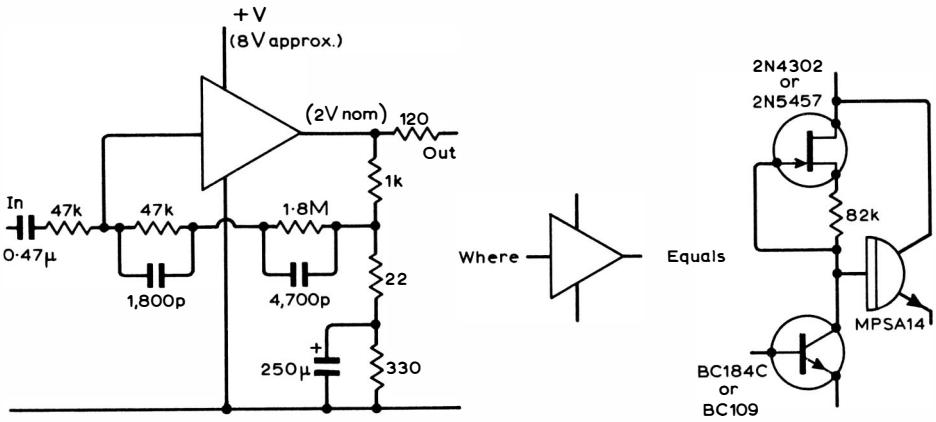
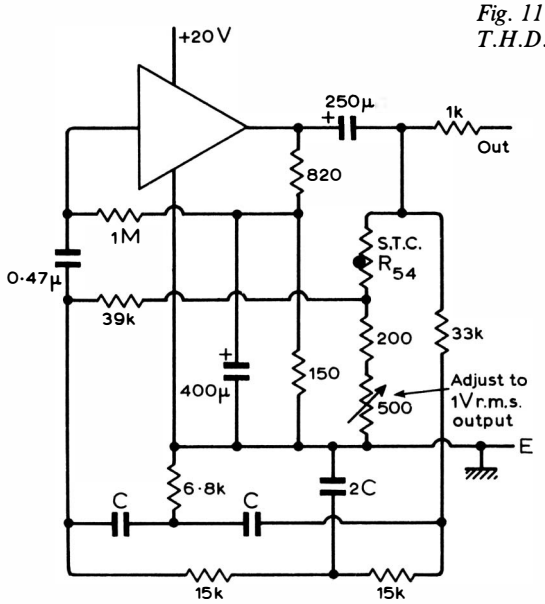


Fig. 10. Very low noise, low-distortion magnetic pickup input equalization stage. Z_{in} = 47 kΩ. Gain = 50 at 1 kHz. T.H.D. <0·01% at 0·5 V r.m.s. output at 1 kHz.

Liniac applications

Magnetic pickup (R.I.A.A.) equalising stage. Because of the very high loop gain which can be obtained with this stage, even when a simple bipolar input transistor is employed, a very low noise, low distortion R.I.A.A. characteristic correction circuit can be made with this arrangement giving a gain of 50 at 1 kHz, and less than 0·01% t.h.d. at up to 0·5 V r.m.s. output. A suitable circuit arrangement is shown in Fig. 10.

Low-distortion oscillator. A very low distortion oscillator, employing a pentode valve amplifier, was described by A. R. Bailey in 1960[1]. In this the phase shift in a slightly unbalanced parallel "T" circuit is used to provide the necessary positive feedback to sustain oscillation, with the advantage of very good frequency stability. A circuit based on the same principle, but employing a liniac, is shown in Fig. 11. Since the number of variables is somewhat inconvenient for a continuously variable frequency oscillator, it is suggested that the capacitors should be switched to give a series of fixed frequencies.



C = 0·1μ F = 100Hz
C = 0·5μ F = 200Hz
C = 0·02μ F = 500Hz
C = 0·01μ F = 1kHz
etc.

Fig. 11. Very low distortion oscillator. T.H.D.<0·005% at 1 V r.m.s. output.

The distortion given by the prototypes of this, in the frequency range 200 Hz–5 kHz, is certainly below 0·005% at 1 V r.m.s. output. As such this circuit provides a useful reference standard for testing amplifiers, distortion meters and notch filter circuits. Incidentally the resistors used were normal high-quality carbon-film types, and no advantage was found, in terms of any measurable improvement in distortion, in changing over to wire-wound units as originally recommended by Bailey. However, the performance of the thermistor has been found to have an important influence on the overall distortion figure (of five units tried one was found to worsen the distortion to some 0·05%). It is thought that the electrolytic capacitors should also be of high quality.

Pre-amplifier tone control circuit. The very high gain, high input impedance and low noise and distortion characteristics of this circuit make it a natural choice for a Baxandall-type of negative feedback pre-amplifier tone control circuit, and a suitable arrangement giving approximately 20 dB of bass and treble lift and cut at 40 Hz and 15 kHz with respect to 800 Hz, is shown in Fig. 12. The worst case (maximum lift) distortion of this circuit is better than 0·02% at

1 V r.m.s. output. This is at least 20 times better than the conventional (and very widely used) single transistor circuit under similar worst case conditions.

Other circuits using Darlington transistors

F.E.T.—bipolar feedback pair. Because of the relatively high output impedance of the normal grounded-source junction f.e.t. amplifier, it is not possible to construct f.e.t.

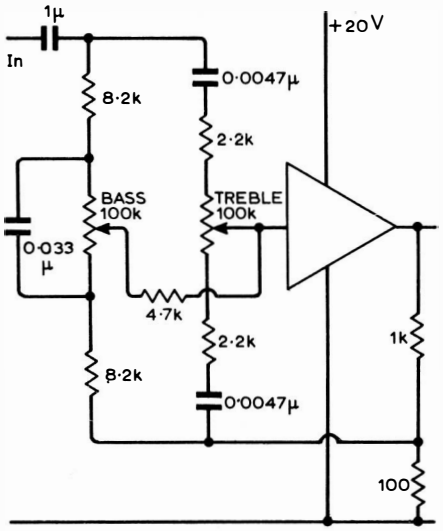
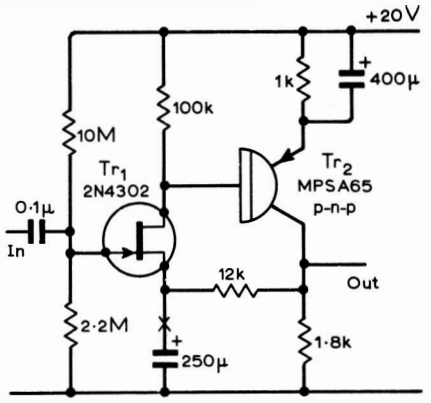


Fig. 12. Liniac employed in tone control stage. Max. output 3 V r.m.s. Source impedance ⩽ 10 kΩ. Midpoint gain 10× ±18 dB lift/cut at 50 Hz and 15 kHz w.r.t. 800 Hz. Worst case t.h.d. <0·02%.

—bipolar feedback pairs of a form analogous to the excellent circuit arrangements typified by Figs. 1(b) and 1(c), without the overall gain being much reduced by the inevitable mismatch at the drain of the f.e.t. However, if the second transistor is a Darlington device, the mismatch is avoided, and open loop gains of 4000× are feasible, in the non-inverting mode. The circuit arrangements is shown in Fig. 13. For comparison, the same circuit with a 2N4058 or BC214 as Tr_2 has only a gain of 100.

Improved bipolar feedback pair. The circuit of Fig. 2(b) can itself be improved by the use of a Darlington transistor as Tr_2. The use of an MPSA65 p-n-p device gives loop gains in excess of 6000, for example. A suitable circuit of this general type is shown in Fig. 14.



Feedback resistor inserted at X to provide feedback control of gain

Open loop gain ≃ 4,000

Fig. 13. F.E.T./Darlington pair. High-gain high-input impedance.

D.C. bootstrap circuit. The fact that the emitter of a Darlington transistor will follow the base signal level very accurately, with a constant potential difference of about 1 V, allows the connection of a load resistor between the base and emitter as shown in Fig. 15, which multiplies the effective dynamic impedance of the resistor at all frequencies down to d.c. by a figure which approaches the Darlington transistor current gain. The f.e.t. amplifier circuit has a gain of about 250.

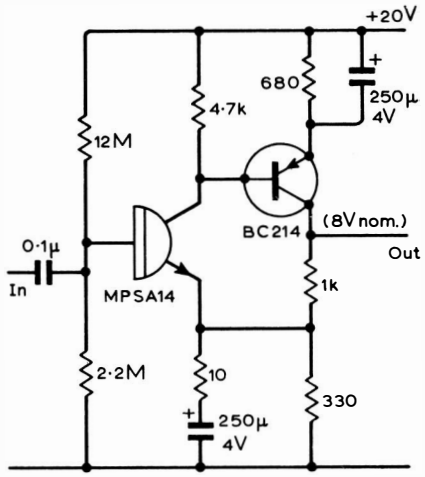


Fig. 14. Improved bipolar transistor feedback pair. $Z_{in} \approx 1{\cdot}5\ M\Omega$. Gain ≈ 100.

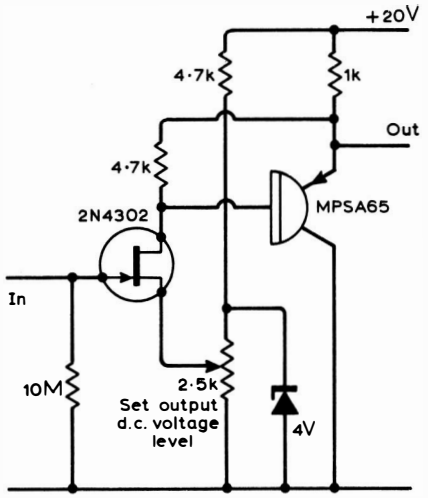


Fig. 15. D.C. bootstrap circuit (phase inverting). Gain ≈ 250.

Inexpensive plastic encapsulated and other relatively low-cost devices of this type are available from Motorola, Fairchild, SGS, and GE. Type numbers are MPSA 12, 13 and 14, BFX 66 and 67, and D16P4 for n-p-n types; and MPSA 65 and 66 (Motorola) for p-n-p devices. The MPSA 12 Motorola unit is a low noise pre-amp type.

Reference

1. Bailey, A. R., *Electronic Technology*, Feb. 1960, pp. 64–67. www.keith-snook.info

H.F. Predictions—September

Solar activity is now steadily declining as this table of Ionospheric Index IF2 shows.

	1966	1969	1971
Jan.	15	95	94
Feb.	21	104	85
Mar.	33	127	83
Apr.	37	122	74
May	46	118	70
June	55	119	(70)
July	55	114	(68)
Aug.	53	122	(65)
Sept.	42	115	(63)
Oct.	47	110	(59)
Nov.	64	106	(57)
Dec.	66	108	(55)

Forecast values are given in brackets. The years 1969 and 1970 were almost identical and constitute the maximum of the current sunspot cycle. A minimum is expected in 1975.