DESIGN YOUR OWN PROJECTS

No.4

IMPEDANCE MATCHING AMPLIFIER

TOBY BAILEY & BOB WHITAKER

This month we are going to take a look at the solution to a simple problem which covers some very important points, many of which we have not really considered in previous projects in this series. The background to this project is that a little while ago we went to visit a friend who, seeing us arrive, gestured wildly from his window for us to be quiet and then came out to meet us. The reason for this charade turned out to be that he was trying to copy a tape from a reel-to-reel machine to a cassette recorder. The problem was that the output socket of the first machine was inadequate to drive the input of the second. He was solving this problem by recording from loudspeaker to microphone!

Now one doesn't need to be a dedicated Hi-Fi fanatic to realise that this is a horribly unsatisfactory way of recording, for more reasons than the inhospitality it creates so we resolved to settle the problem electronically.

Specification

A little delving around in the typically inadequate booklets supplied by the manufacturers of the machines revealed that we needed an amplifier with a voltage gain of about ten, an input impedance of at least 20kΩ and an output impedance of less than 5kΩ. Choosing a supply voltage of 9 volts which should prove to be a simple and practical value, completes the basic specification.

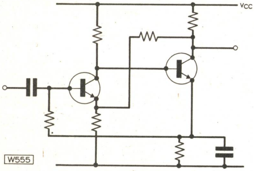

Fig. 1: A typical "feed-back pair".

With regard to the type of circuit that we are going to base the rest of our design on, the next thing to consider is whether a two-stage transistor amplifier is necessary or whether one stage is sufficient. The great advantage of "feedback pair" arrangements such as the one shown in **Fig. 1** is that you effectively "design out" the transistor characteristics by using masses of feedback. The reason for doing this is that the essential characteristics of the circuit are then almost independent of the parameters of the individual transistors used, which may vary quite a bit between individual specimens. These characteristics are then dependent on the passive components present.

Is it possible to achieve this desirable state of affairs using only one transistor? Well, the real reason that the circuit shown in **Fig. 1** works is that the two transistors used have a much higher gain than that of the overall circuit, this gain being settled by the feedback network. As the gain of a single transistor common emitter stage is in principle a couple of hundred and since we only want a gain of ten there seems to be plenty of scope for producing a stable circuit using negative feedback. The reader may well be acquainted with the technique that we are going to employ, but possibly does not recognise it as feedback.

Feedback

There are essentially two ways to apply negative feedback to a one transistor stage; these are shown in **Fig. 2**. Although both of these circuits stabilise the gain they differ in many respects—it is useful to have some idea of why this is so. First let us look at the series version shown in **Fig. 2(a)**. The operation is fairly simple: when the base voltage rises a little the collector current increases, however this means that the emitter current increases as well which causes the emitter voltage to rise. The total effect is that the emitter voltage tends to "follow" the base voltage and hence the voltage difference between the base and the emitter doesn't change nearly as much as the base voltage itself does. The result of all this is that the voltage gain is reduced and the input impedance is increased. Putting these facts in terms of formulae: the voltage gain becomes RL/Re and the input impedance is hFE x Re in parallel with the bias resistors. We should point out in passing that these formulae are at best only approximate and cease to be valid if you are overly ambitious and try to produce more gain than the transistor can provide. In particular a resistance of 25/Ie (where Ie is the emitter current in mA) should be put in series with Re for the purpose of both the above calculations. The circuit should be fed from a source with a low output impedance compared with the input-impedance, otherwise the feedback will not work as intended. The operation of the shunt feedback arrangement shown in **Fig. 2(b)** is entirely different. Here we require a high impedance source and the idea is to make the signal current taken by the base of the transistor negligible compared with that flowing in RF and the signal source. Under these conditions the current gain becomes Rf/RL and the voltage gain from the unloaded source to output is then Rf/Rs where Rs is the source resistance. This is essentially a current amplifier and the feedback will not be realised unless the source is a current source i.e. has a high internal impedance.

It is fairly clear that our application is one that requires a voltage amplifier and so we will base our design on the circuit of **Fig. 2(a)**. Given the basic framework of the circuit, let us now proceed with the detailed design.

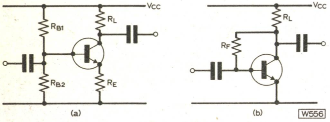

Fig. 2: Series and shunt feed-back circuits.

Design

The first thing to do is to decide on the static (i.e. DC) voltages and currents and select a suitable transistor. In the higher echelon of the designing business it is normal to design the circuit, find out what specifications are needed for the transistor and then select the transistor type from the multitudes available. It is a lot easier here to say that we will use a BC109 because it has high gain, low noise, and is readily available. Readers who have ever looked up data on the BC109 will have found that most of it is given for a collector current of 2mA, but 1mA seems quite adequate for this job. Our supply voltage is 9V and it is sensible to space out our collector and emitter voltages as much as possible so as to have a large margin for possible error. Lets settle for an emitter voltage of 2·7V and a collector voltage of 9−2·7=6·3V. This means that we will require a base voltage of about 2·7+0·6=3·3V. This stage of the design is shown in **Fig. 3**: all that we have used here is Ohm's Law and the well known facts that the forward bias on the base-emitter junction of a silicon transistor is about 0·6V and that the emitter and collector currents will have about the same value.

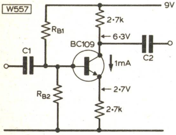

Fig. 3: Initial voltage requirements.

Bias Network

The time has now come to assign values to RB1 and RB2. There is a rule of thumb which states that the current flowing down the resistor chain should

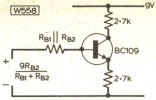

Fig. 4: Bias network equivalent circuit.

be at least five times, and preferably ten times, the maximum base current. There is, however, a much better way of calculating the resistor values: this involves regarding the bias network as a simple voltage source with an internal resistance. In our case the voltage is given by $\frac{9RB2}{RB1 + RB2}$ and its internal impedance is RB1 in parallel with RB2 (written RB1 ‖ RB2). An equivalent circuit of the bias network is shown in **Fig. 4**. We must now decide how great we can allow this source impedance to be. Now the static DC gain (hFE) of a BC109 at Ic=2mA is quoted as 200-800, so let us play safe and assume a value of 150. In this case the maximum base current

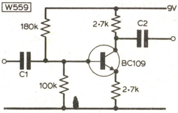

Fig. 5: The potential divider values.

is going to be 1/150 mA. It is probably quite safe to let this have the effect of dropping the bias voltage by half a volt, so we set a maximum on RB1 ‖ RB2 of

$$\frac{1}{2} \div \frac{1}{150}\,\text{k}\Omega = 75\text{k}\Omega.$$ So we want a potential divider which produces a voltage of about 3·3V off load and which has an impedance of about 75kΩ. A calculation reveals that RB1=180kΩ and RB2=100kΩ satisfy these conditions and have a source impedance of about 64kΩ. If you calculate it yourself you will find that these values give almost exactly five times the current in the divider as is expected in the base, confirming the value of the rule of thumb approach. The method that we have used is, however, more instructive and is applicable to cases when there are several different supply rails. Anyway, back to business: we have now reached the stage shown in **Fig. 5**.

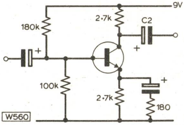

Fig. 6: Decoupling added to modify impedance.

Gain and Impedance

It is now time to look at the voltage gain of our circuit. At the moment it is just less than one, so to realise our aim of a gain of ten at audio frequencies we will need to reduce the impedance to AC signals at the collector. This is done with a decoupling capacitor. We have already mentioned that the gain

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is the ratio of the load resistance to the impedance in the emitter so for a gain of ten we want, to be on the safe side, the AC impedance at the collector to be about 200Ω. We already have 25/Ie=25Ω internally which we mentioned earlier, so 180Ω in series with a capacitor should be fine (see **Fig. 6**). As for the value of the capacitor, we want its impedance to be small compared with the 180Ω for the lowest frequency at which we want the circuit to operate. If we take this frequency to be 30Hz, and say that the impedance should be about 20Ω at 30Hz then we have, using the expression for the impedance of a capacitor,

$$X = \frac{1}{2\pi fC}$$

$$20 = \frac{1}{2\pi 30C} \quad \text{so} \quad C = \frac{1}{1200\pi}$$

so a value of 250μF should be adequate.

Now for a check of the input impedance of the circuit. This is given by the input impedance of the transistor in parallel with the bias network. We said before that the transistor's input impedance is hFE x Re. hFE for the BC109 should be at least 200, so this becomes 40kΩ. Now 40kΩ in parallel with 64kΩ (the bias network) will give a value well over the 20kΩ required by the specification, so we're OK here. We can easily allow C1 to have a value of 2kΩ at our

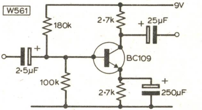

Fig. 7: The completed circuit of the matching amplifier.

low frequency limit, so anything over about 2·5μF should be adequate. At the output it seems reasonable to let C2 have an impedance of about 20Ω at 30Hz so this gives C2=25μF. The final design is shown in **Fig. 7.**