LOW-DRIFT/LOW-NOISE dc AMPLIFIER

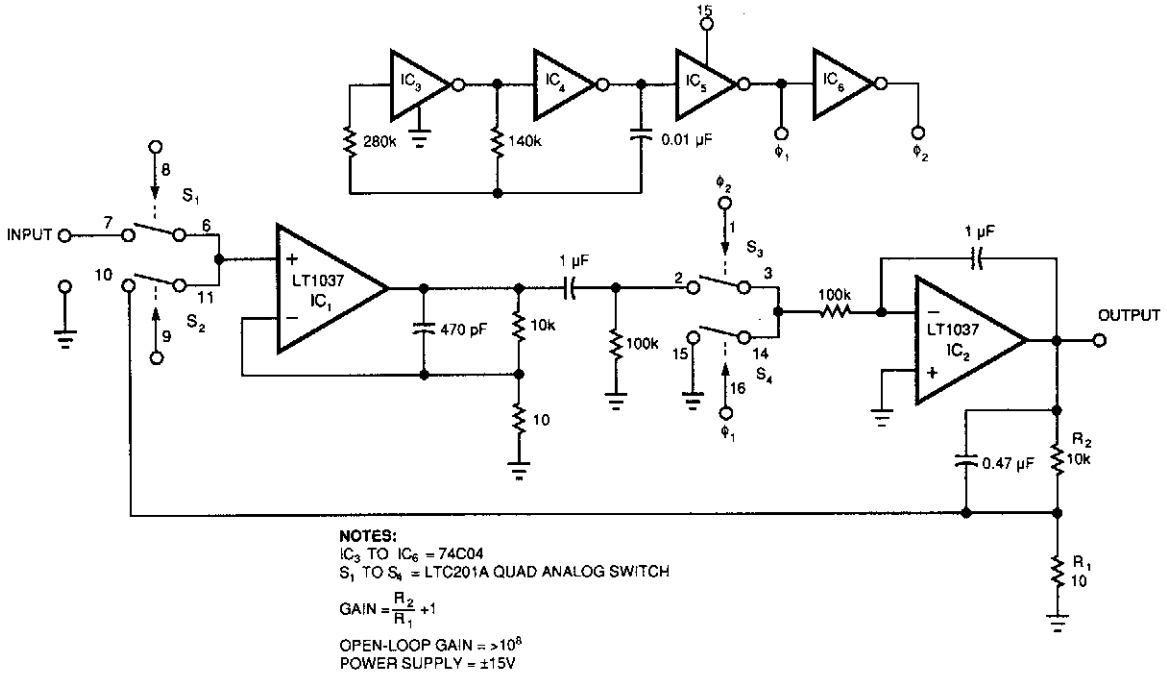

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Fig. 39-2

Figure 39-2's circuit combines a low-noise op amp, IC1, with a chopper-based carrier-modulation scheme to achieve a low-noise, low-drift dc amplifier whose performance exceeds any currently available monolithic amplifier. The amplifier's offset is less than 1 μV, and its drift is less than 0.05 μV/°C. This circuit has noise within a 10-Hz bandwidth less than 40 nV. The amplifier's bias current, which is set by the bipolar input of IC1, is about 25 nA.

The 74C04 inverters (IC3 to IC6) form a simple 2-phase square-wave clock that runs at about 350 Hz. The complementary oscillator signals (O_1 and O_2) provide drive to S1 and S2, respectively, causing a chopped version of the input to appear at IC1's input. IC1 amplifies this ac signal. S3 and S4 synchronously demodulate IC1's square-wave output. Because S3 and S4 switch synchronously with S1 and S2, the circuit presents proper amplitude and polarity information to IC2, the dc output amplifier. This output stage integrates the square wave to provide a dc voltage output. R1 and R2 divide the output and feed it back to the input chopper where the divided output serves as a zero signal reference. The ratio of R1 and R2 sets the gain, in this case to 1 000.