

ASUS CONFIDENTIAL

MODEL NAME : Elsa
PCB NO : ???
ASUS P/N : ???

Lanai UMA Schematics Document

uFCPGA Mobile Merom
Intel Crestline-GM + ICH8M

2007-03-19

REV :1.2(DELL: X02)

MB PCB	
Part Number	Description
DA800004H0L	PCB 00B LA-3071P REV0 MB

BOM NO. ???
PCB P/N: ???

PROJECT:	REVISION	DATE: Monday, March 19, 2007	DESCRIPTION: Cover Page	SCHMATIC FILE NAME :	DESIGN ENGINEER :
	1.2	SHEET OF 68		RELEASE DATE :	

LANAI: UMA

CLOCK
CK410M+LP
PG 21

POWER

POWER SEQUENCE LOGIC PG 51
POWER CHARGER PG 57
POWER CONTROL SWITCH PG 49
DISCHARGE PATH PG 49 +3.3V_SUS/+5V_SUS/+3.3V_RUN +5V/+3.3V/+1.8V/+1.25V_RUN

Merom
(478 Micro-FCPGA)
PG 7,8
(Symbol Rev.09)

POWER

POWER I/O +1.5V_RUN/+1.05V_VCCP PG 55	POWER VCORE PG 53
REGULATOR +VCC_GFX_CORE/+1.25V_RUN PG 58	POWER SYSTEM 5V_ALW & 3.3V_ALW PG 54
	REGULATOR +1.8V_SUS/+0.9V_DDR_VTT PG 56

Panel Connector
PG 28

Crestline
1299 uFCBGA
PG 9,10,11,12,13,14
(Symbol Rev.09)

533/667 MHZ DDR II

DDR2-SODIMM1
PG 19

533/667 MHZ DDR II

DDR2-SODIMM2
PG 19

IO Board

CRT CONN.	VGA	D.B CON PG 50
TV CONN.	TVOUT	
USB CONN.x2	USB2.0(P2,3)	
MINI-CARD WLAN	PCIEx1 (Lane2)	
MINI-CARD WWAN	USB2.0(P9)	

ICH8-M
676 BGA
PG 15,16,17,18
(Symbol Rev.09)

SIM CARD Board

AUDIO/AMP
PG 44,45,46

MDC
PG 36

S/PDIF TO TV CONN.
PG 30

DIGITAL MIC.
PG 28

Speaker CON
PG 46

WtoB CON
PG 46

Audio Jacks *3

JACK Board

RJ11 Board

USB2.0(P0,P1) -> USB CONN. PG 39 -> USB Board

PCIE (Lane6)

PCI

PCIE (Lane4)

USB2.0(P6)

USB2.0(P7)

USB2.0(P5)

CAMERA PG 28

SATA

IDE

SATA-HDD PG 31

CD-ROM PG 31

Bluetooth PG 41

CARD READER 1394/R5C833 PG 32,33,34

BCM5906KMLG QFN-68 PG 47

RJ45/Magnetic PG 48

EXPRESS-CARD R5538 PG 35

SIO MEC5025 128KB Flash TMKBC 128 Pins VTQFP PG 37

SIO ECE5011 Expander USB 2.0 Hub(4) 128 Pins VTQFP PG 38

CIR PG 41

FLASH PG 40

Touchpad CON. PG 41

FAN & THERMAL EMC4001 PG 43

USER INTERFACE PG 42

SNIFFER PG 42

CAPBTN CON. PG 40

PROJECT:	REVISION	DATE: Monday, March 19, 2007	DESCRIPTION:	SCHEMATIC FILE NAME :	DESIGN ENGINEER :
	1.2	SHEET OF 68	BLOCK DIAGRAM	RELEASE DATE :	

Footprint Definition	
Resistor	Footprint is 0402 if there is no description
Capacitor	Footprint is 0402 if there is no description
Ferrite Bead	Footprint is 0603 if there is no description

Layout Note

For all of ESD diode, they should be placed as close as possible to connectors and the signals from connectors should be routed to ESD diodes first. There is no branch or via before diodes

PCI TABLE			
PCI DEVICE	IDSEL	REQ#/GNT#	PIRQ
R5C833	PCI_AD17	PCI_REQ1# PCI_GNT1#	PCI_PIRQC# PCI_PIRQD#

PCI Express TABLE	
Lane 1	WWAN / Mini Card
Lane 2	WLAN / Mini Card
Lane 3	
Lane 4	ExpressCard
Lane 5	
Lane 6	LAN BCM5906KMLG

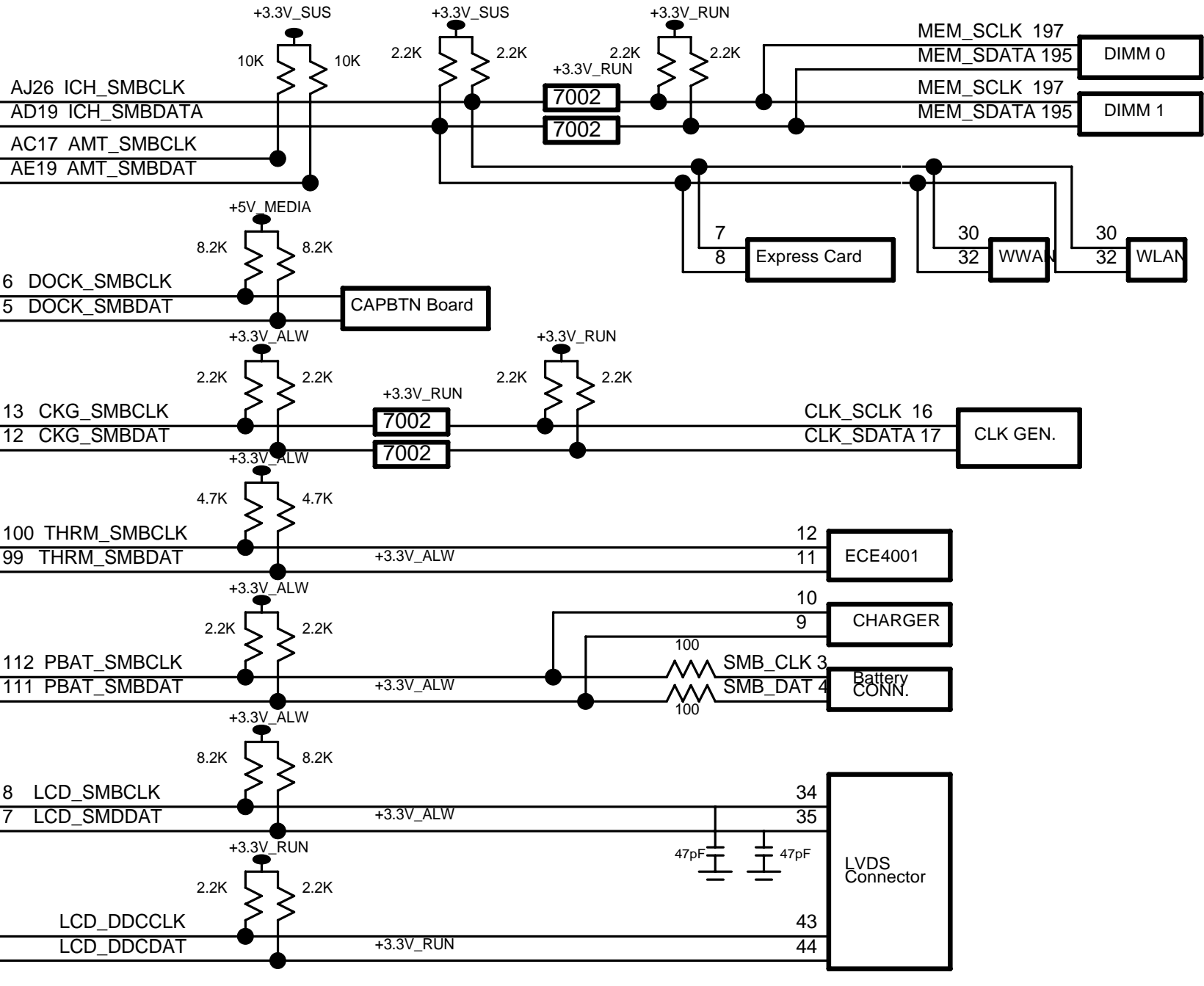
USB TABLE	
ICH8-0 (EHC#1)	User1 (Single port , in USB BD)
ICH8-1 (EHC#1)	User2 (Single port , in USB BD)
ICH8-2 (EHC#1)	User3 (Dual port-bottom , in I/O BD)
ICH8-3 (EHC#1)	User4 (Dual port-top , in I/O BD)
ICH8-4 (EHC#1)	
ICH8-5 (EHC#1)	Camera
ICH8-6 (EHC#2)	ExpressCard
ICH8-7 (EHC#2)	BT Module
ICH8-8 (EHC#2)	
ICH8-9 (EHC#2)	WWAN / Mini Card

Note : No USB for WLAN

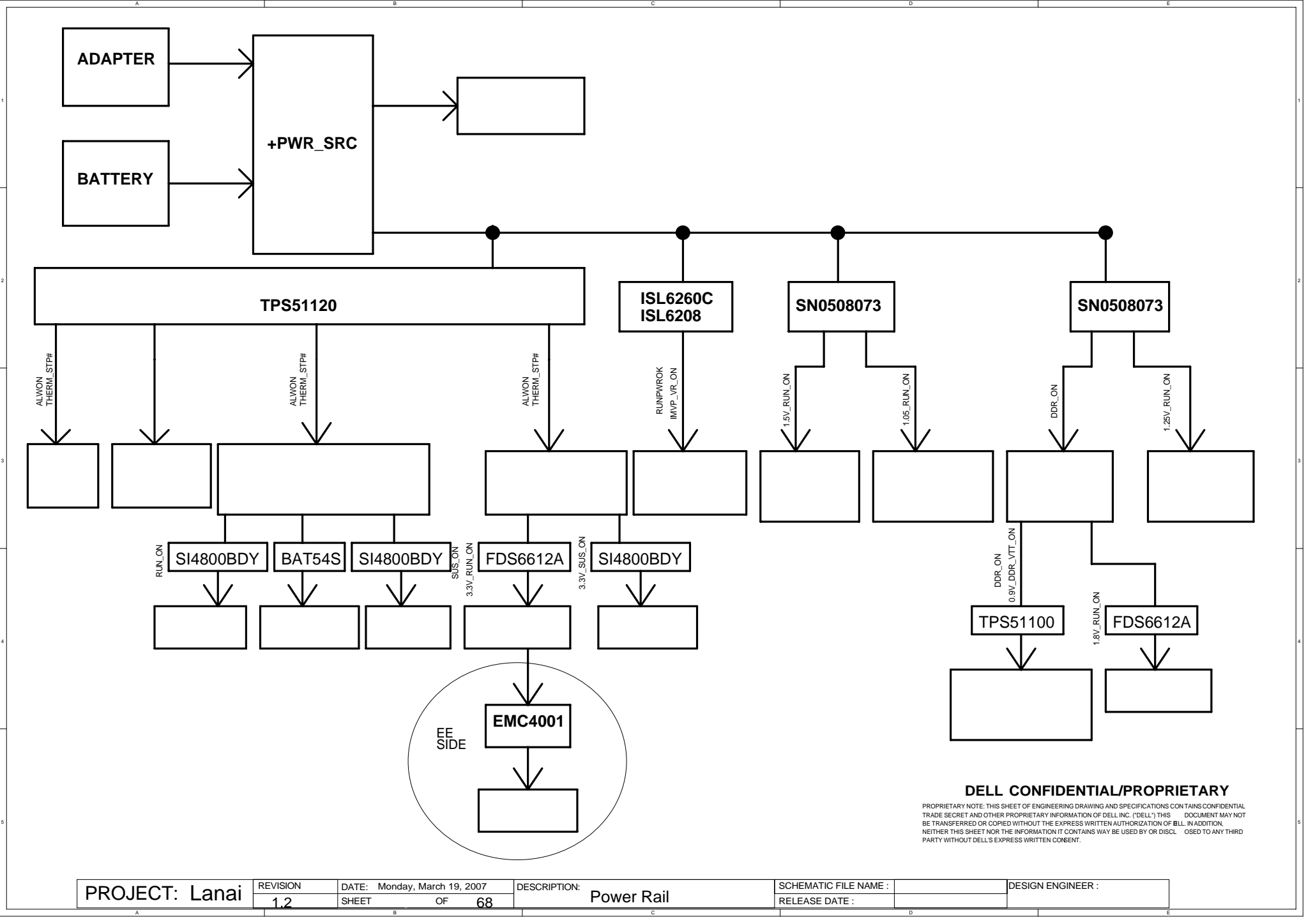
ICH8-M

SIO
MEC5025

VGA



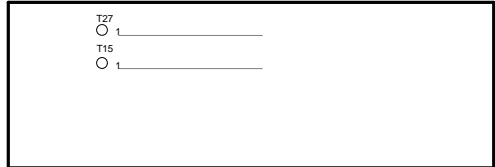
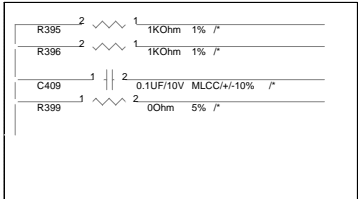
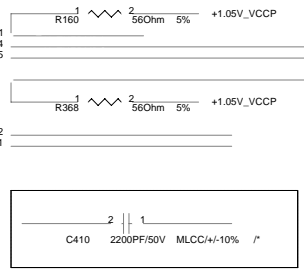
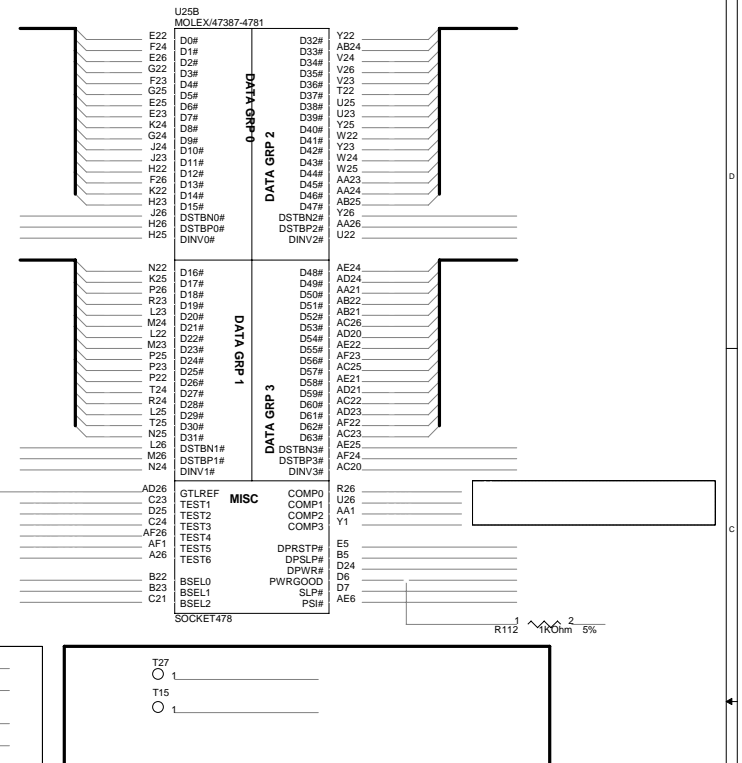
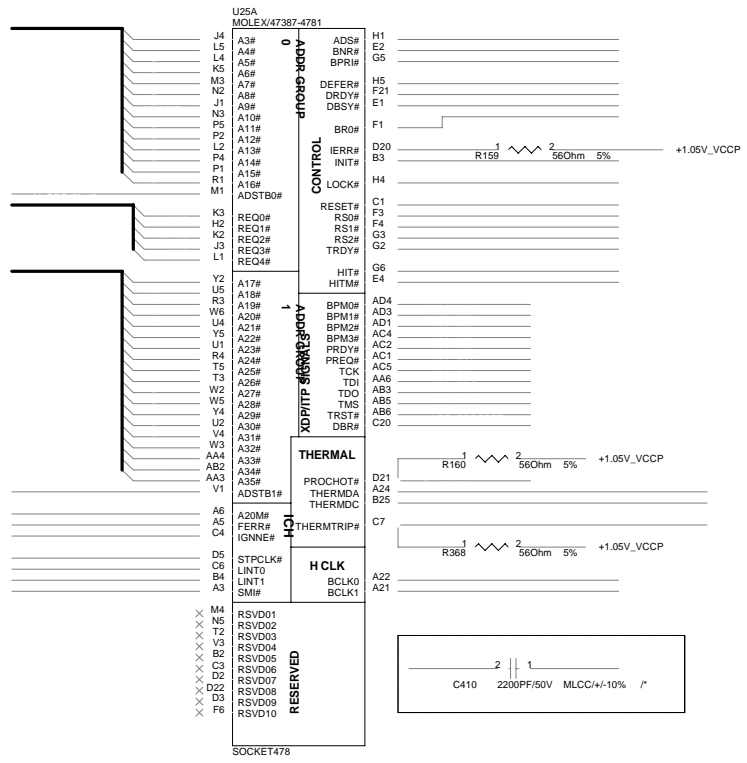
PROJECT: Lanai	REVISION	DATE: Monday, March 19, 2007	DESCRIPTION:	SCHMATIC FILE NAME :	<OrgName>	DESIGN ENGINEER :
	1.2	SHEET OF 68	SMBUS BLOCK	RELEASE DATE :		



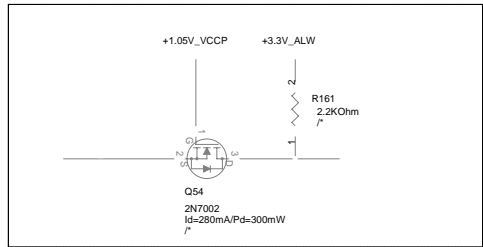
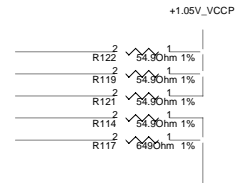
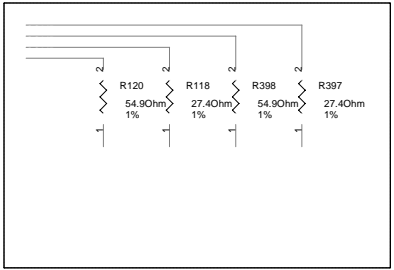
DELL CONFIDENTIAL/PROPRIETARY

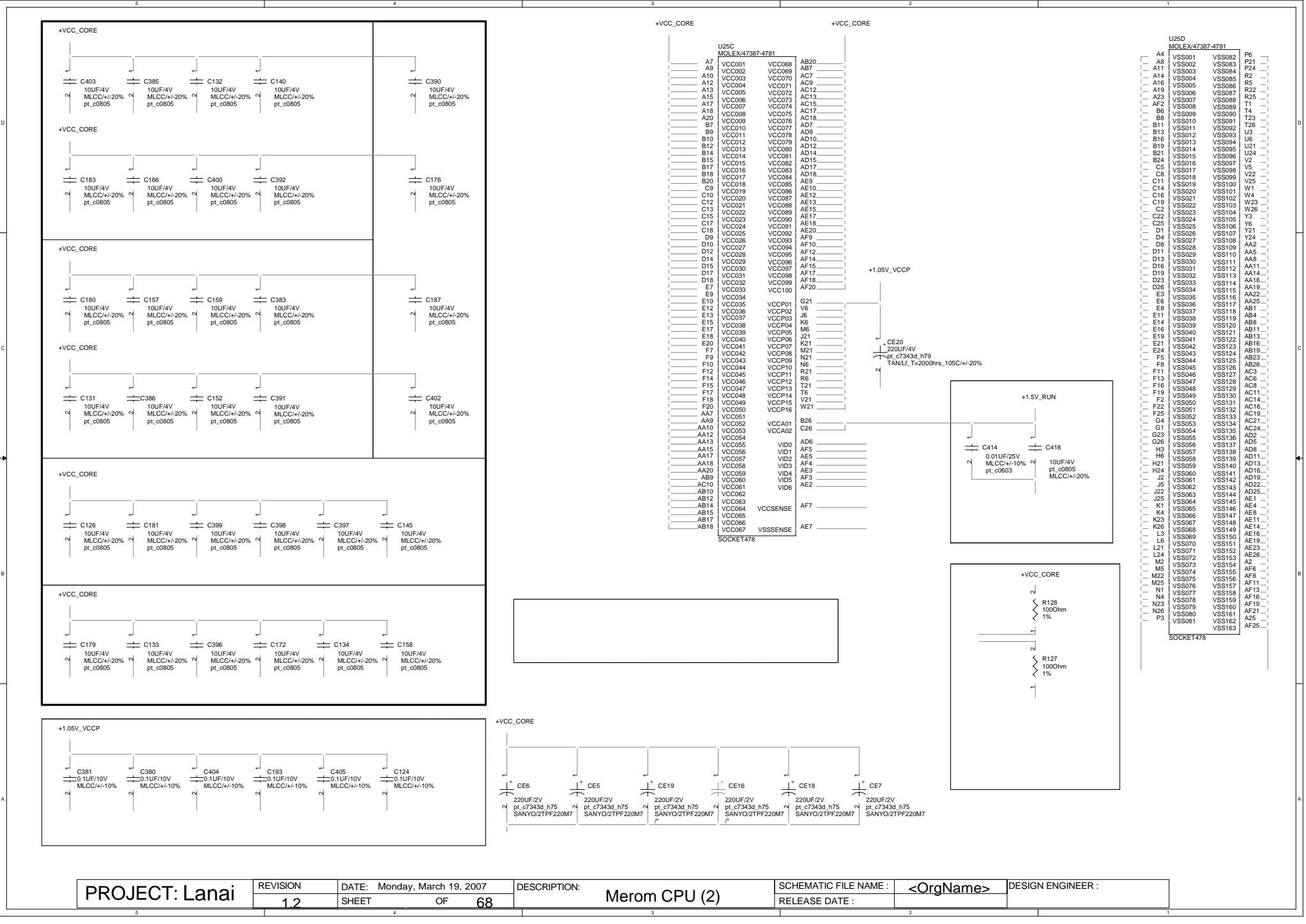
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PROJECT: Lanai	REVISION 1.2	DATE: Monday, March 19, 2007	DESCRIPTION: Power Rail	SCHEMATIC FILE NAME :	DESIGN ENGINEER :
	SHEET OF 68			RELEASE DATE :	

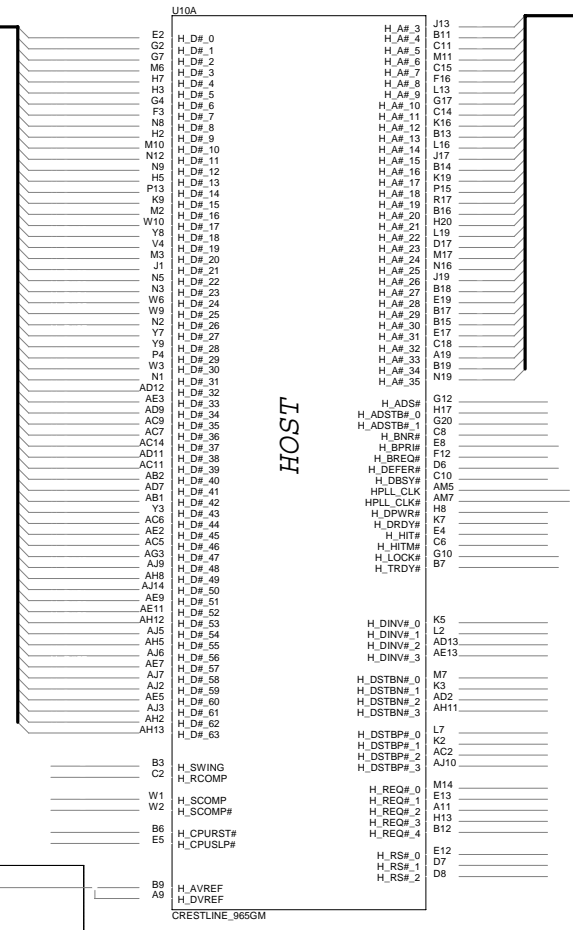
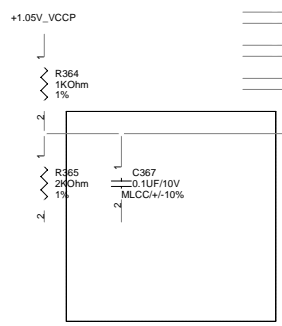
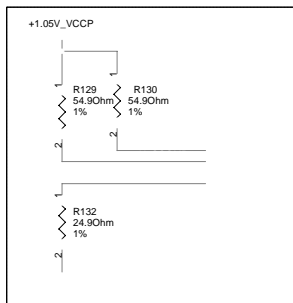
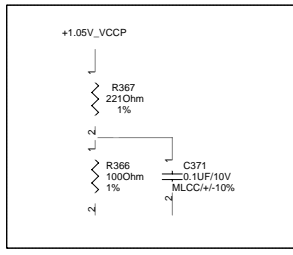


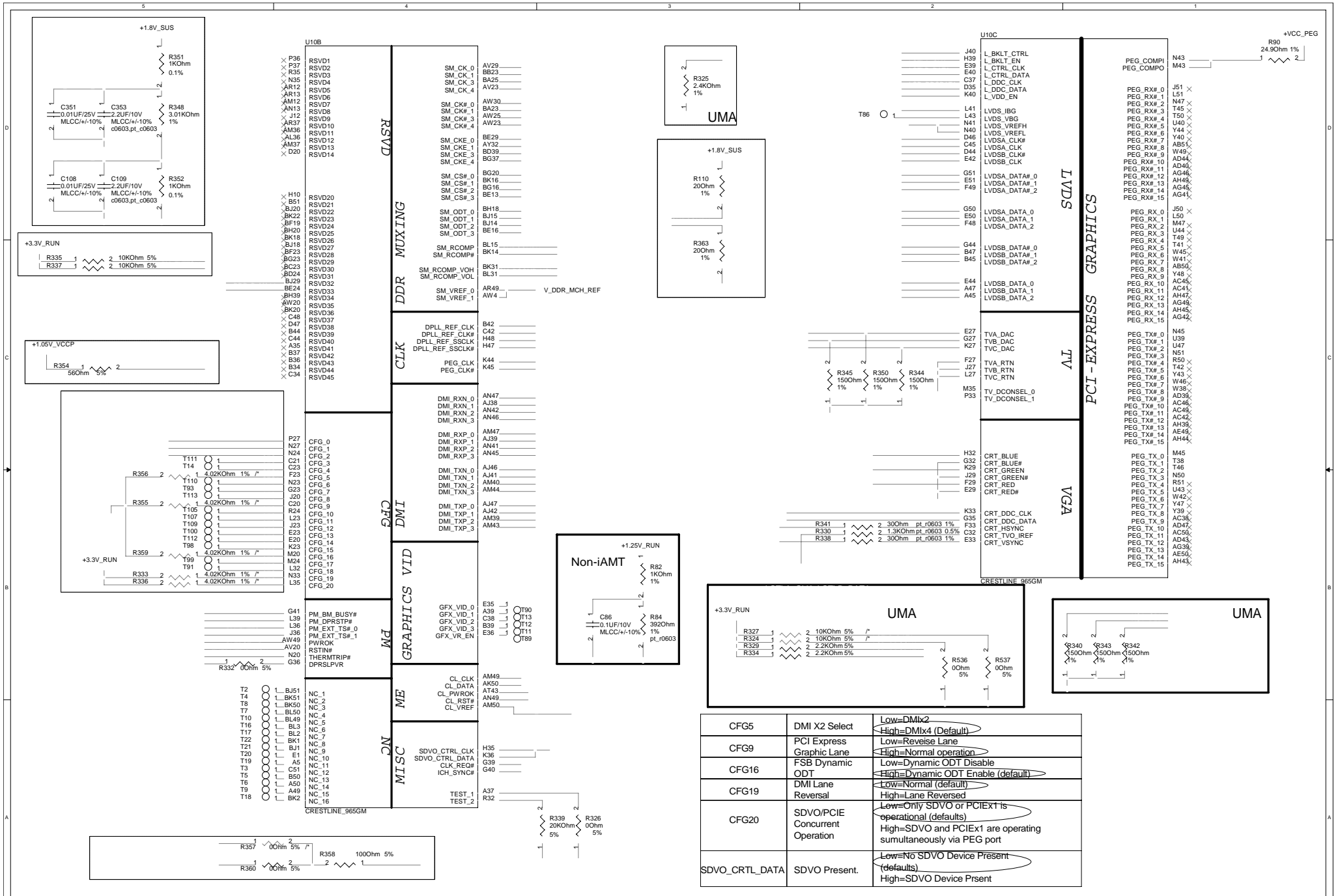
FSB	BCLK	BSEL2	BSEL1	BSEL0
533	133	0	0	1
667	166	0	1	1
800	200	0	1	0



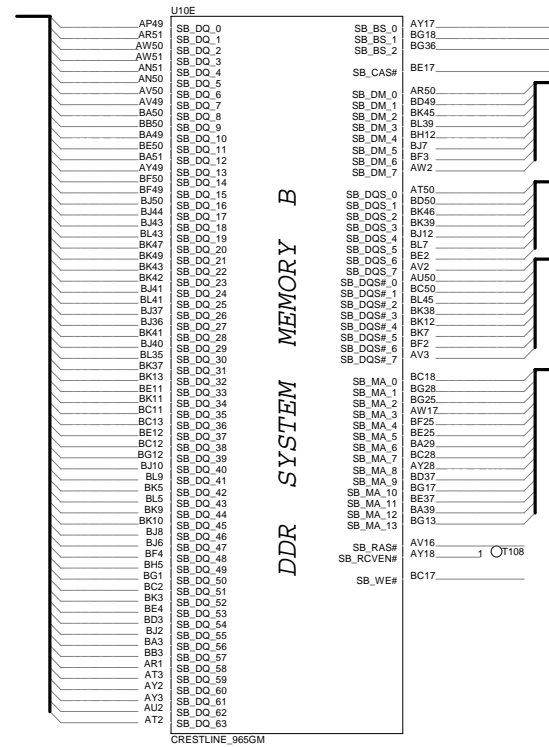
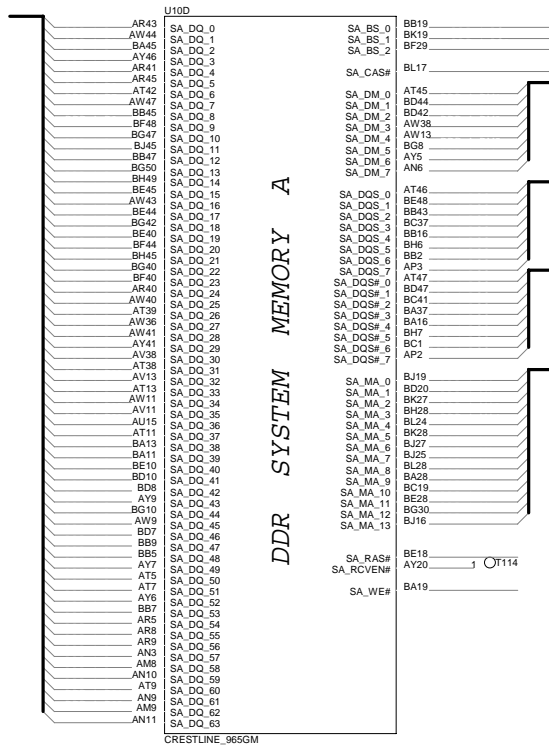


PROJECT: Lanai	REVISION	DATE: Monday, March 19, 2007	DESCRIPTION:	SCHEMATIC FILE NAME :	DESIGN ENGINEER :
	1.2	SHEET OF 68	Merom CPU (2)	<OrgName>	
				RELEASE DATE :	

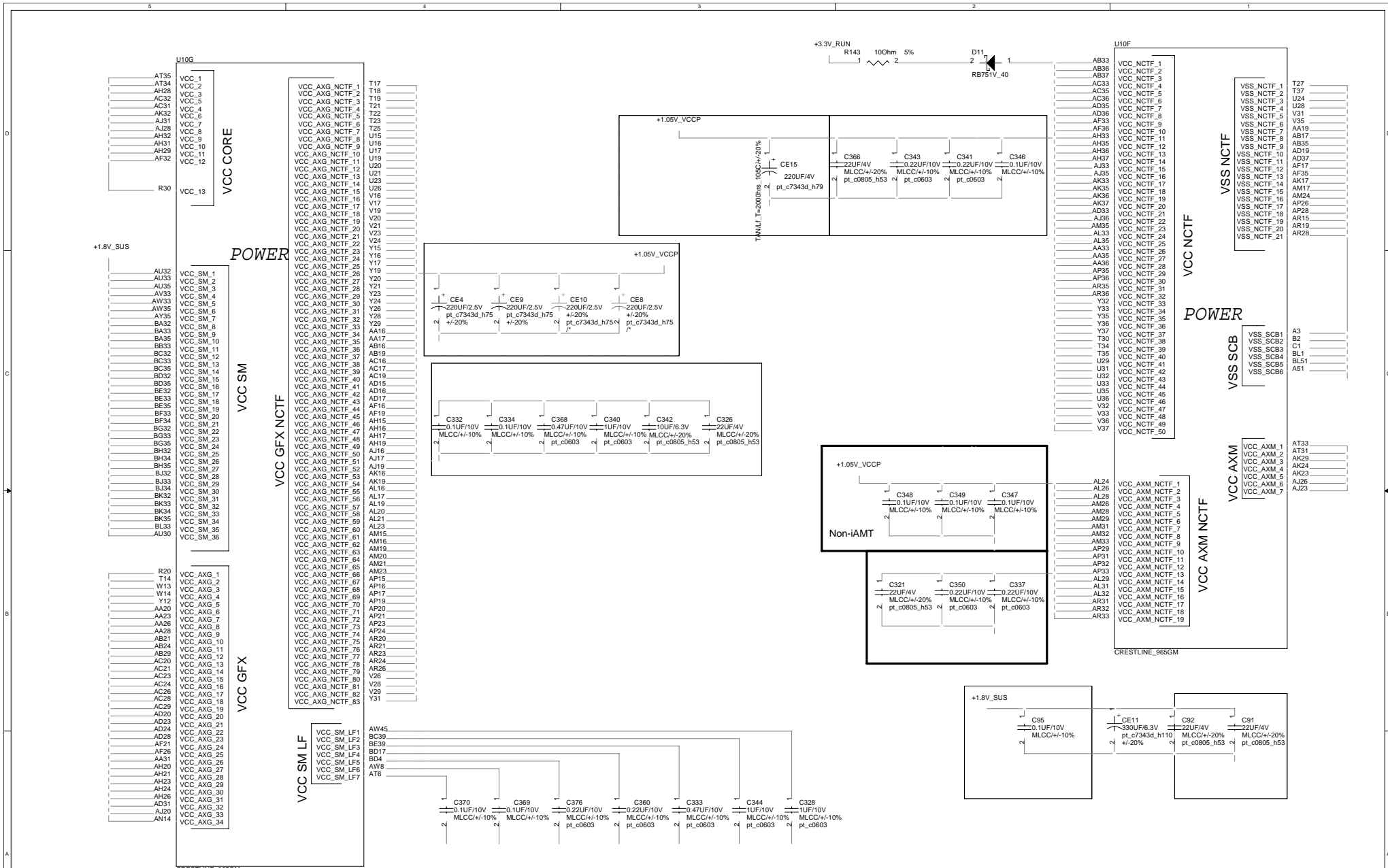




CFG5	DMI X2 Select	Low=DMIx2 High=DMIx4 (Default)
CFG9	PCI Express Graphic Lane	Low=Reverse Lane High=Normal operation
CFG16	FSB Dynamic ODT	Low=Dynamic ODT Disable High=Dynamic ODT Enable (default)
CFG19	DMI Lane Reversal	Low=Normal (default) High=Lane Reversed
CFG20	SDVO/PCIe Concurrent Operation	Low=Only SDVO or PCIEX1 is operational (defaults) High=SDVO and PCIEX1 are operating simultaneously via PEG port
SDVO_CRTL_DATA	SDVO Present.	Low=No SDVO Device Present (defaults) High=SDVO Device Present

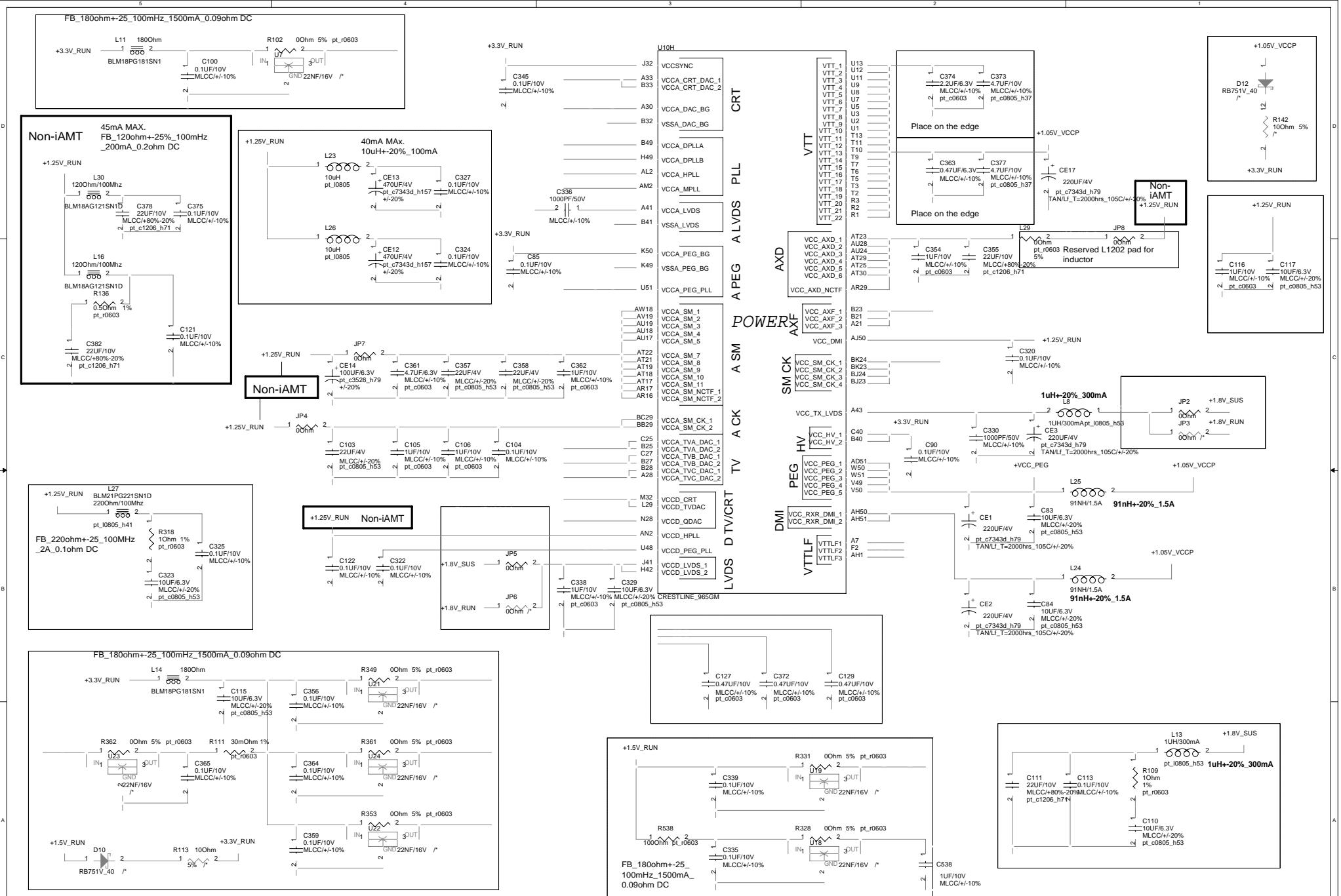


PROJECT: Lanai	REVISION	DATE: Monday, March 19, 2007	DESCRIPTION:	SCHMATIC FILE NAME :	DESIGN ENGINEER :
	1.2	SHEET OF 68	Crestline(DDR2)	<OrgName>	
				RELEASE DATE :	



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PROJECT: Lanai	REVISION	DATE: Monday, March 19, 2007	DESCRIPTION:	SCHEMATIC FILE NAME:	DESIGN ENGINEER:
	1.2	SHEET OF 68	Crestline(VCC,NCTF)	<OrgName>	
				RELEASE DATE:	



PROJECT: Lanai	REVISION	DATE: Monday, March 19, 2007	DESCRIPTION:	SCHMATIC FILE NAME:	DESIGN ENGINEER :
	1.2	SHEET OF 68	Crestline(POWER)	<OrgName>	
RELEASE DATE :					

U101

A13	VSS_1	VSS_100	AW24
A15	VSS_2	VSS_101	AW29
A17	VSS_3	VSS_102	AW32
A24	VSS_4	VSS_103	AW5
AA21	VSS_5	VSS_104	AW7
AA24	VSS_6	VSS_105	AY10
AA29	VSS_7	VSS_106	AY24
AB20	VSS_8	VSS_107	AY37
AB23	VSS_9	VSS_108	AY42
AB26	VSS_10	VSS_109	AY43
AB28	VSS_11	VSS_110	AY45
AB51	VSS_12	VSS_111	AY47
AC10	VSS_13	VSS_112	AY50
AC13	VSS_14	VSS_113	B10
AC3	VSS_15	VSS_114	B20
AC39	VSS_16	VSS_115	B24
AC43	VSS_17	VSS_116	B29
AC47	VSS_18	VSS_117	B30
AD1	VSS_19	VSS_118	B35
AD21	VSS_20	VSS_119	B38
AD26	VSS_21	VSS_120	B43
AD29	VSS_22	VSS_121	B46
AD3	VSS_23	VSS_122	B5
AD4	VSS_24	VSS_123	B4
AD45	VSS_25	VSS_124	BA1
AD49	VSS_26	VSS_125	BA17
AD5	VSS_27	VSS_126	BA18
AD50	VSS_28	VSS_127	BA2
AD8	VSS_29	VSS_128	BA24
AE10	VSS_30	VSS_129	BB12
AE14	VSS_31	VSS_130	BB25
AE6	VSS_32	VSS_131	BB40
AF20	VSS_33	VSS_132	BB49
AF23	VSS_34	VSS_133	BB8
AF24	VSS_35	VSS_134	BB8
AF31	VSS_36	VSS_135	BC16
AG2	VSS_37	VSS_136	BC24
AG38	VSS_38	VSS_137	BC5
AG43	VSS_39	VSS_138	BC36
AG47	VSS_40	VSS_139	BC40
AG50	VSS_41	VSS_140	BC51
AH3	VSS_42	VSS_141	BD13
AH40	VSS_43	VSS_142	BD2
AH41	VSS_44	VSS_143	BD28
AH7	VSS_45	VSS_144	BD45
AH9	VSS_46	VSS_145	BD48
AJ11	VSS_47	VSS_146	BD5
AJ13	VSS_48	VSS_147	BE1
AJ21	VSS_49	VSS_148	BE19
AJ24	VSS_50	VSS_149	BE23
AJ29	VSS_51	VSS_150	BE30
AJ32	VSS_52	VSS_151	BE42
AJ43	VSS_53	VSS_152	BE51
AJ45	VSS_54	VSS_153	BE8
AJ49	VSS_55	VSS_154	BF12
AK20	VSS_56	VSS_155	BF16
AK21	VSS_57	VSS_156	BF36
AK26	VSS_58	VSS_157	BG19
AK28	VSS_59	VSS_158	BG2
AK31	VSS_60	VSS_159	BG24
AL1	VSS_61	VSS_160	BG29
AL11	VSS_62	VSS_161	BG39
AM11	VSS_63	VSS_162	BG48
AM13	VSS_64	VSS_163	BG5
AM3	VSS_65	VSS_164	BG51
AM4	VSS_66	VSS_165	BH17
AM41	VSS_67	VSS_166	BH30
AM45	VSS_68	VSS_167	BH44
AN1	VSS_69	VSS_168	BH46
AN38	VSS_70	VSS_169	BH8
AN39	VSS_71	VSS_170	BJ11
AN43	VSS_72	VSS_171	BJ13
AN5	VSS_73	VSS_172	BJ38
AN7	VSS_74	VSS_173	BJ4
AP4	VSS_75	VSS_174	BJ42
AP48	VSS_76	VSS_175	BJ46
AP50	VSS_77	VSS_176	BK15
AR11	VSS_78	VSS_177	BK17
AR2	VSS_79	VSS_178	BK25
AR39	VSS_80	VSS_179	BK29
AR44	VSS_81	VSS_180	BK36
AR47	VSS_82	VSS_181	BK40
AR7	VSS_83	VSS_182	BK44
AT10	VSS_84	VSS_183	BK6
AT14	VSS_85	VSS_184	BK8
AT41	VSS_86	VSS_185	BL11
AT49	VSS_87	VSS_186	BL13
AU1	VSS_88	VSS_187	BL19
AU23	VSS_89	VSS_188	BL22
AU29	VSS_90	VSS_189	BL37
AU3	VSS_91	VSS_190	BL47
AU36	VSS_92	VSS_191	C12
AU49	VSS_93	VSS_192	C16
AU51	VSS_94	VSS_193	C19
AV39	VSS_95	VSS_194	C28
AV48	VSS_96	VSS_195	C29
AW1	VSS_97	VSS_196	C33
AW12	VSS_98	VSS_197	C38
AW16	VSS_99	VSS_198	C41

CRESTLINE_965GM

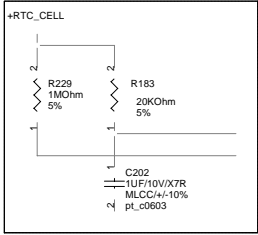
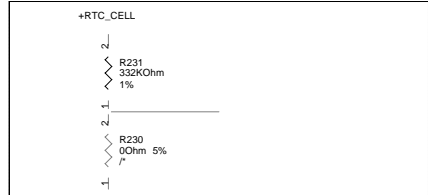
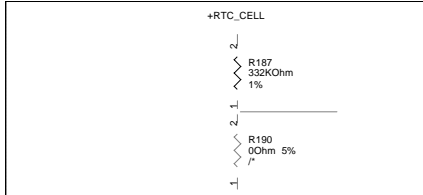
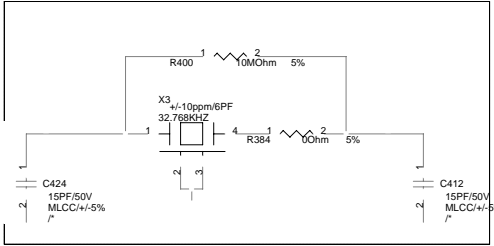
VSS

U101

C46	VSS_199	VSS_287	W11
C50	VSS_200	VSS_288	W39
C7	VSS_201	VSS_289	W43
D13	VSS_202	VSS_290	W47
D24	VSS_203	VSS_291	W5
D3	VSS_204	VSS_292	W7
D32	VSS_205	VSS_293	Y13
D39	VSS_206	VSS_294	Y2
D45	VSS_207	VSS_295	Y41
D49	VSS_208	VSS_296	Y45
E10	VSS_209	VSS_297	Y49
E16	VSS_210	VSS_298	Y5
E24	VSS_211	VSS_299	Y50
E28	VSS_212	VSS_300	Y11
E32	VSS_213	VSS_301	P29
E47	VSS_214	VSS_302	T29
F19	VSS_215	VSS_303	T31
F36	VSS_216	VSS_304	T33
F4	VSS_217	VSS_305	R28
F40	VSS_218		
F50	VSS_219		
G1	VSS_220		
G13	VSS_221	VSS_306	AA32
G16	VSS_222	VSS_307	AB32
G19	VSS_223	VSS_308	AD32
G24	VSS_224	VSS_309	AF28
G28	VSS_225	VSS_310	AF29
G29	VSS_226	VSS_311	AT27
G33	VSS_227	VSS_312	AV25
G42	VSS_228	VSS_313	H50
G45	VSS_229		
G48	VSS_230		
H24	VSS_231		
H28	VSS_232		
H4	VSS_233		
H45	VSS_234		
J11	VSS_235		
J16	VSS_236		
J2	VSS_237		
J24	VSS_238		
J28	VSS_239		
J33	VSS_240		
J35	VSS_241		
J39	VSS_242		
J39	VSS_243		
K12	VSS_245		
K47	VSS_246		
K9	VSS_247		
L1	VSS_248		
L17	VSS_249		
L20	VSS_250		
L24	VSS_251		
L3	VSS_252		
L33	VSS_253		
L49	VSS_254		
M28	VSS_255		
M42	VSS_256		
M46	VSS_257		
M49	VSS_258		
M5	VSS_259		
M50	VSS_260		
M9	VSS_261		
N11	VSS_262		
N14	VSS_263		
N17	VSS_264		
N29	VSS_265		
N32	VSS_266		
N36	VSS_267		
N36	VSS_268		
N39	VSS_269		
N44	VSS_270		
N49	VSS_271		
N7	VSS_272		
P19	VSS_273		
P2	VSS_274		
P23	VSS_275		
P3	VSS_276		
P50	VSS_277		
R49	VSS_278		
T43	VSS_279		
T47	VSS_280		
T47	VSS_281		
U41	VSS_282		
U45	VSS_283		
U50	VSS_284		
V2	VSS_285		
V3	VSS_286		

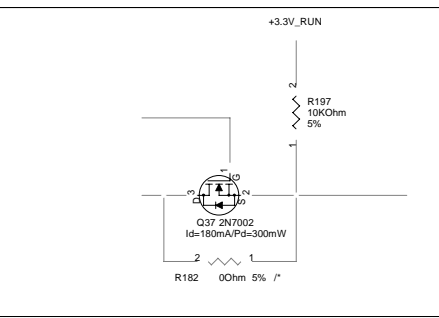
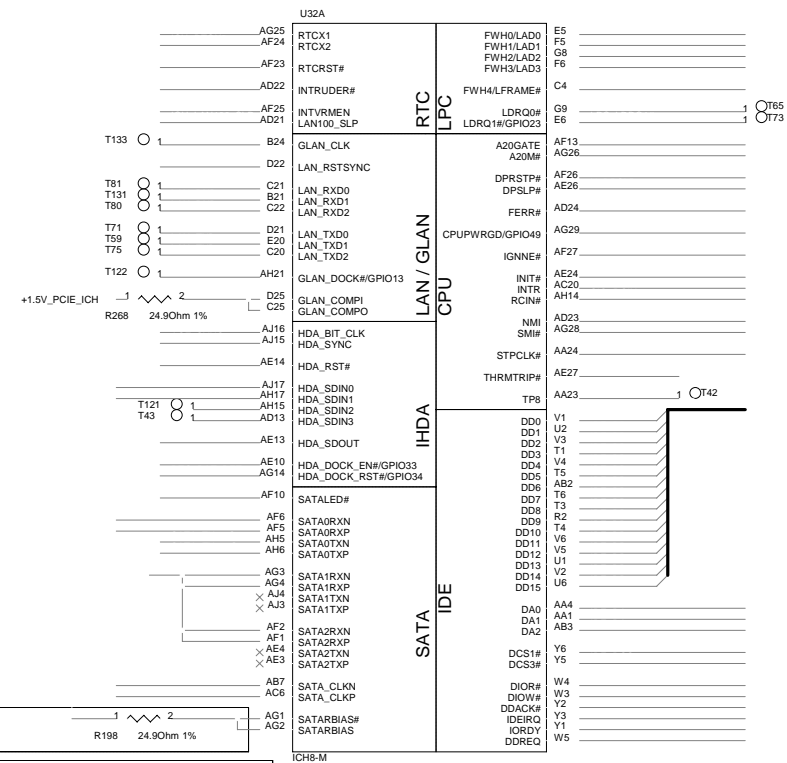
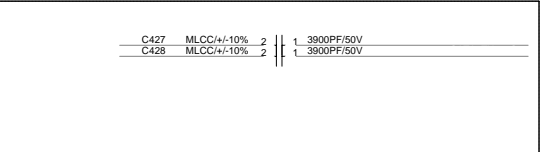
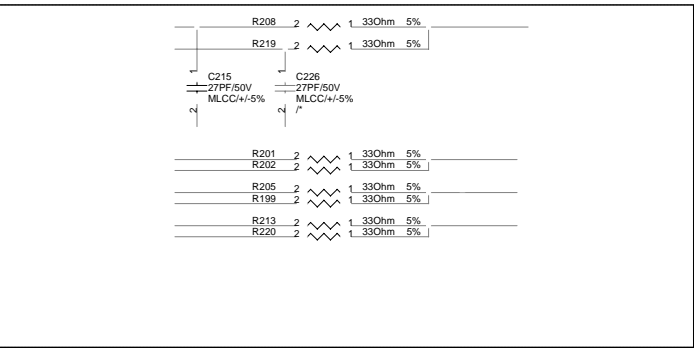
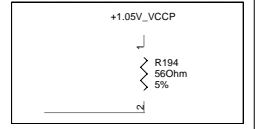
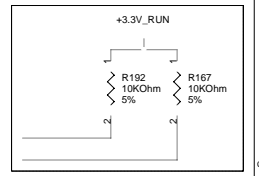
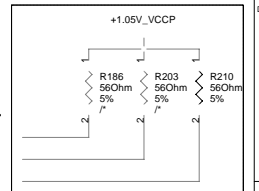
CRESTLINE_965GM

VSS



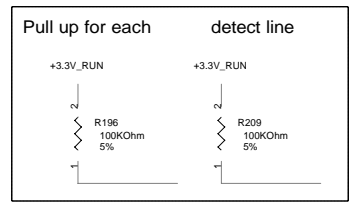
ICH8M Internal VR Enable Strap
(Internal VR for VccSus1.05, VccSus1.5 and VccCL1.5)
 ICH_INTVRMEN Low = Internal VR Disabled
 High = Internal VR Enable(Default)

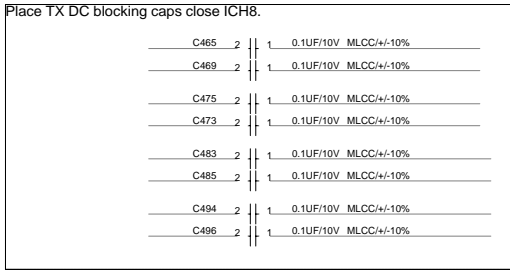
ICH8M LAN100SLP Strap
(Internal VR for VccLAN1.05 and VccCL1.05)
 ICH_LAN100_SLP Low = Internal VR Disabled
 High = Internal VR Enable(Default)



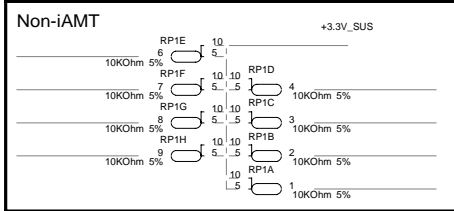
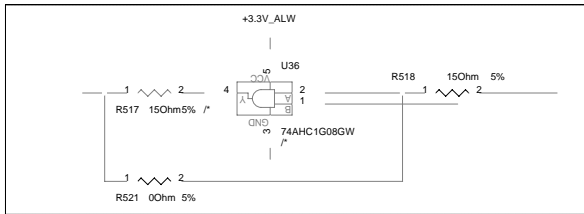
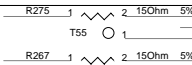
Place within 500 mils of ICH8 ball

XOR Chain Entrance strap		
ICH_RSVD	ACZ_SDOUIT	Description
0	0	RSVD
0	1	Enter XOR chain
1	0	Normal operation (Default)
1	1	Set PCIe port config bit 1

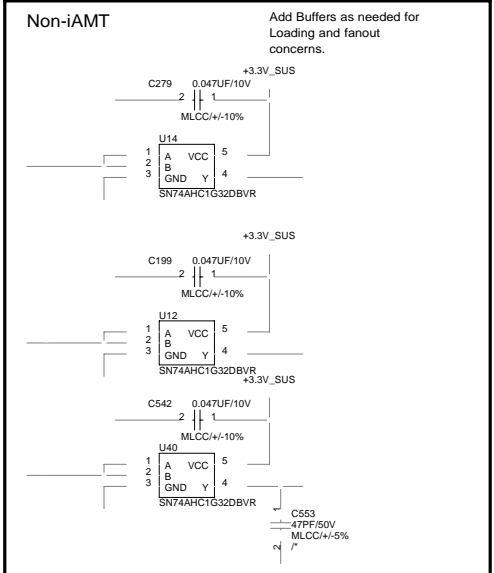
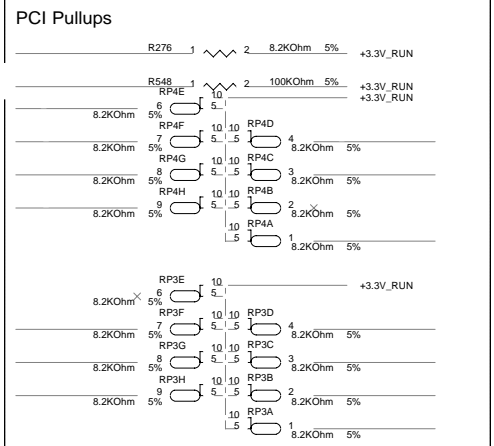
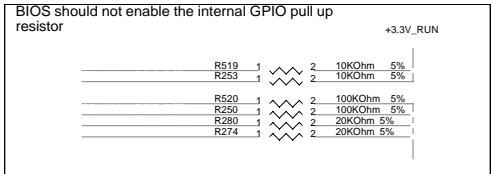
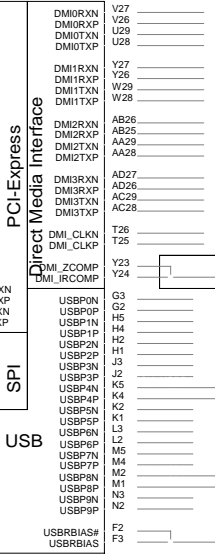
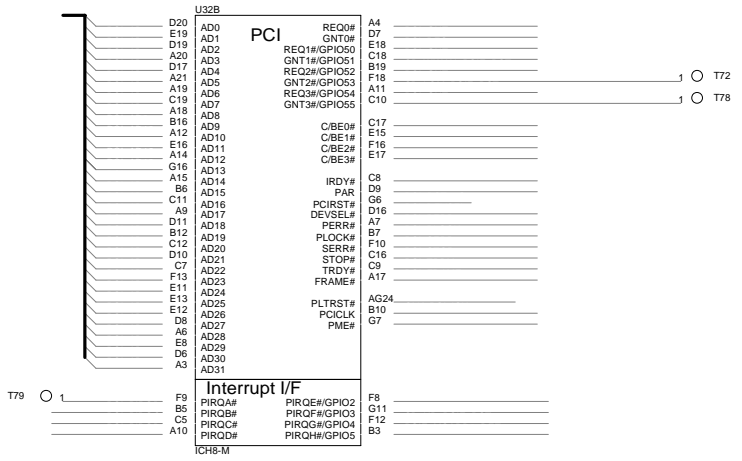
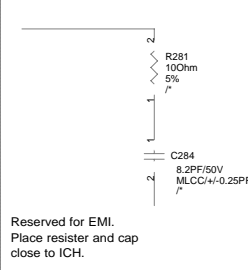
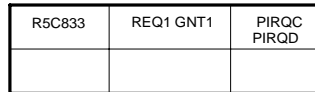
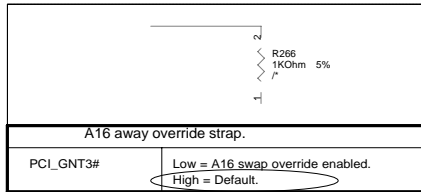
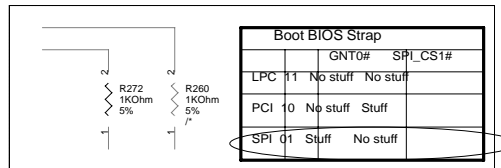




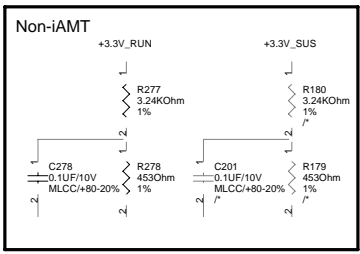
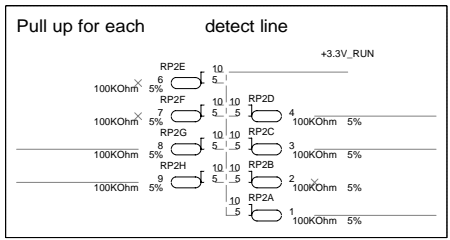
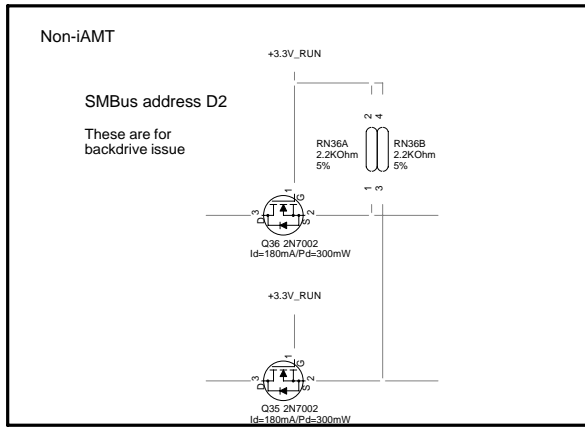
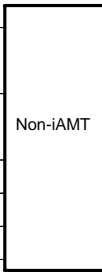
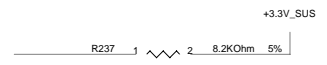
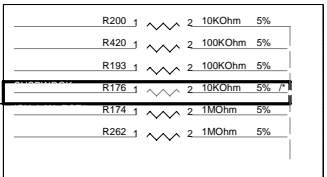
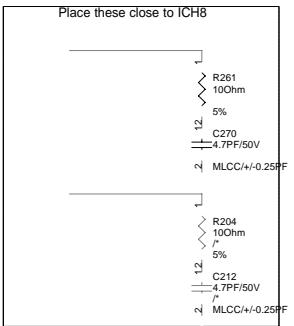
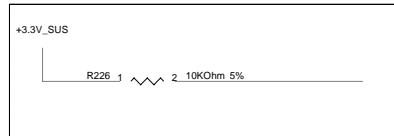
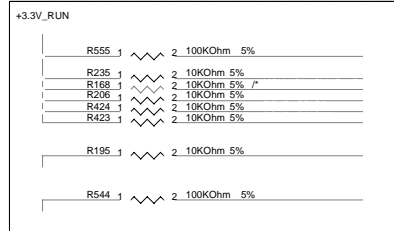
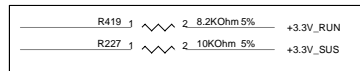
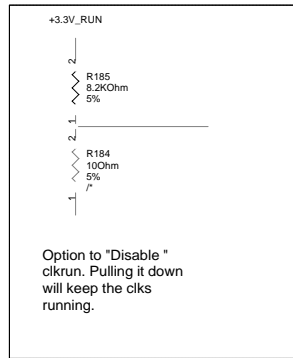
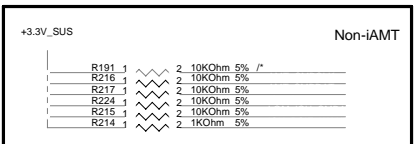
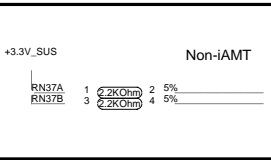
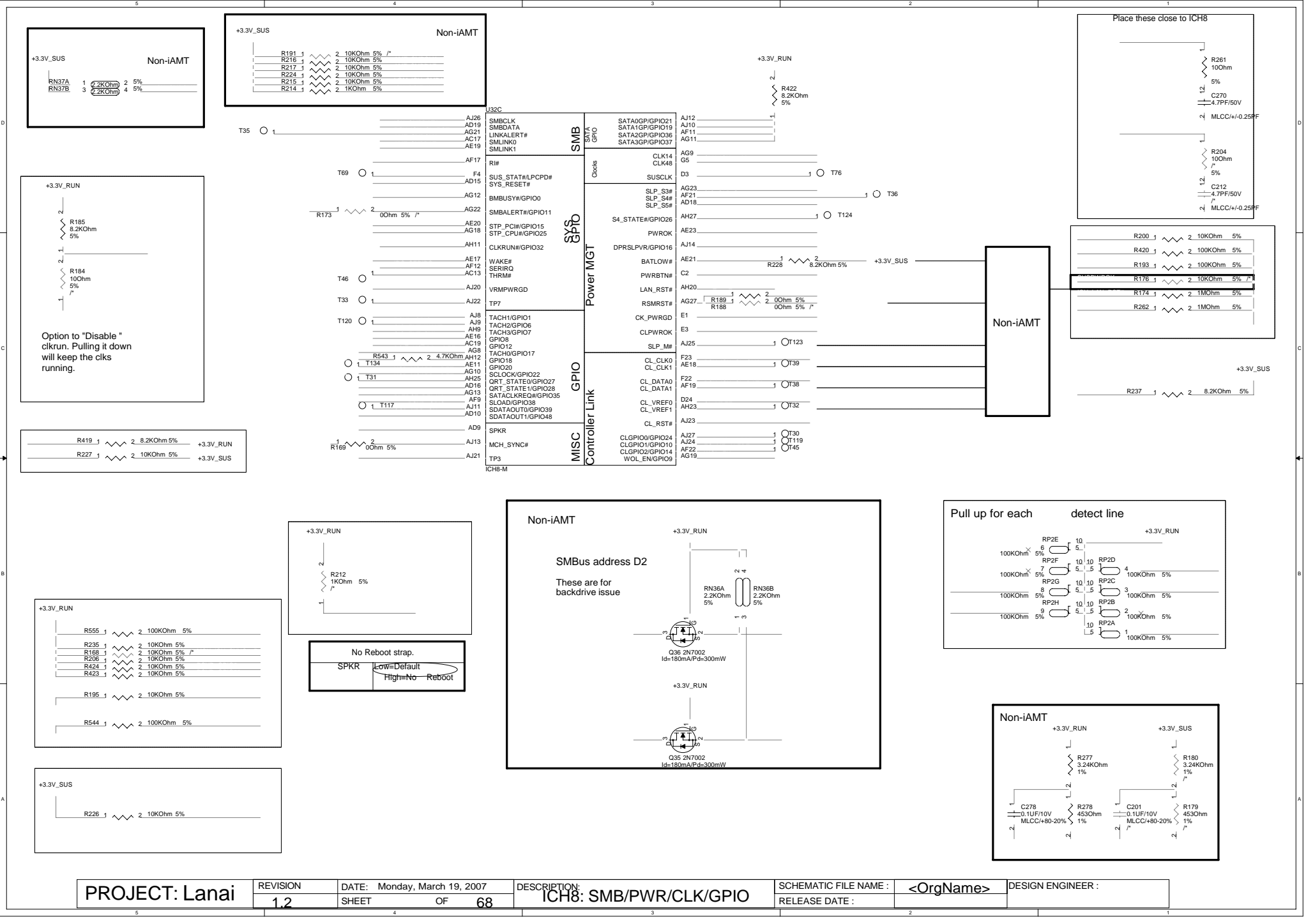
Layout Note:
Place 15 ohm within
500 mils from ICH8.

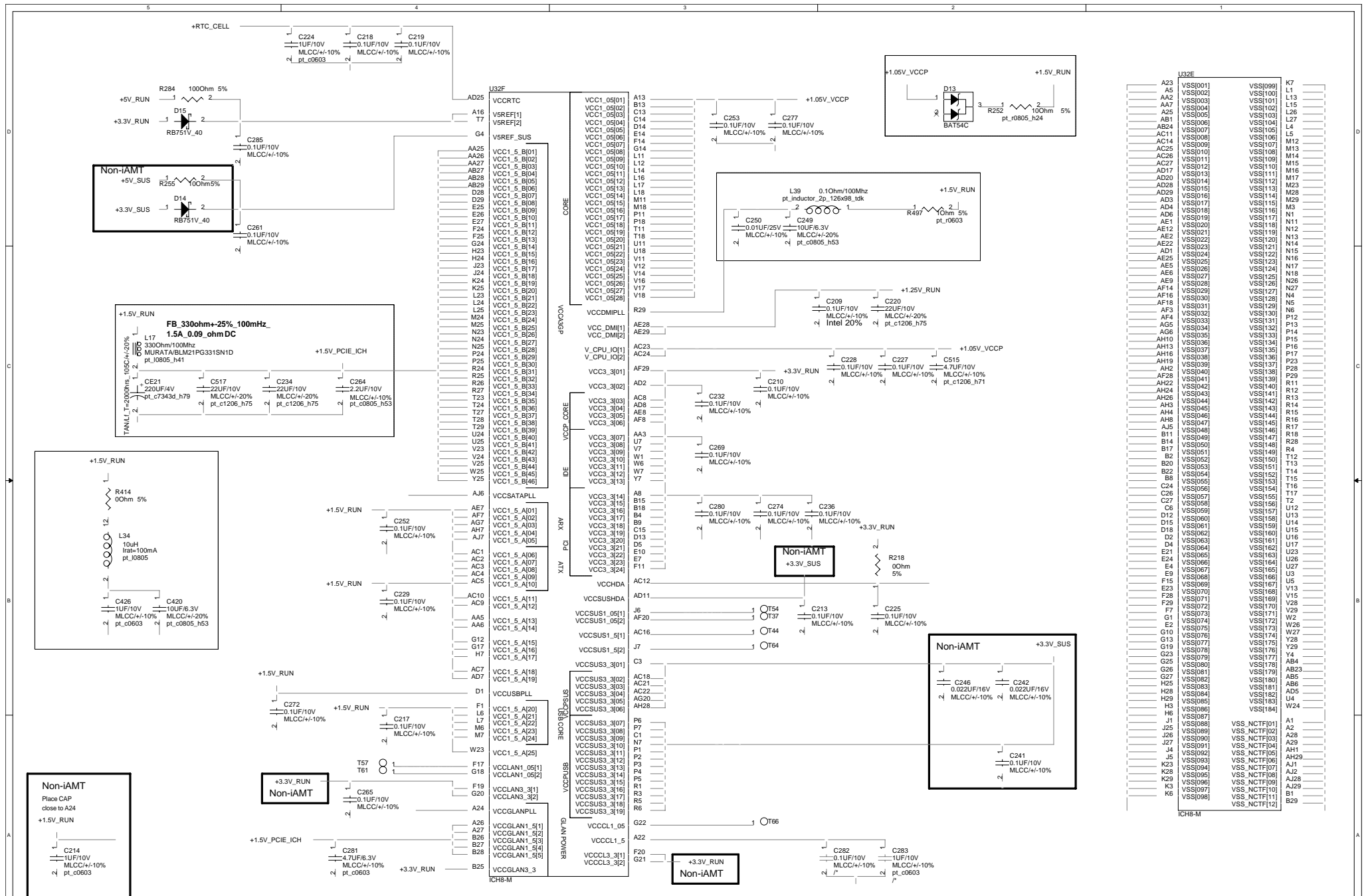


Short F2 and F3 at the package and keep length to less than 500mils. Trace Impedance should be 60ohms +/- 15%.

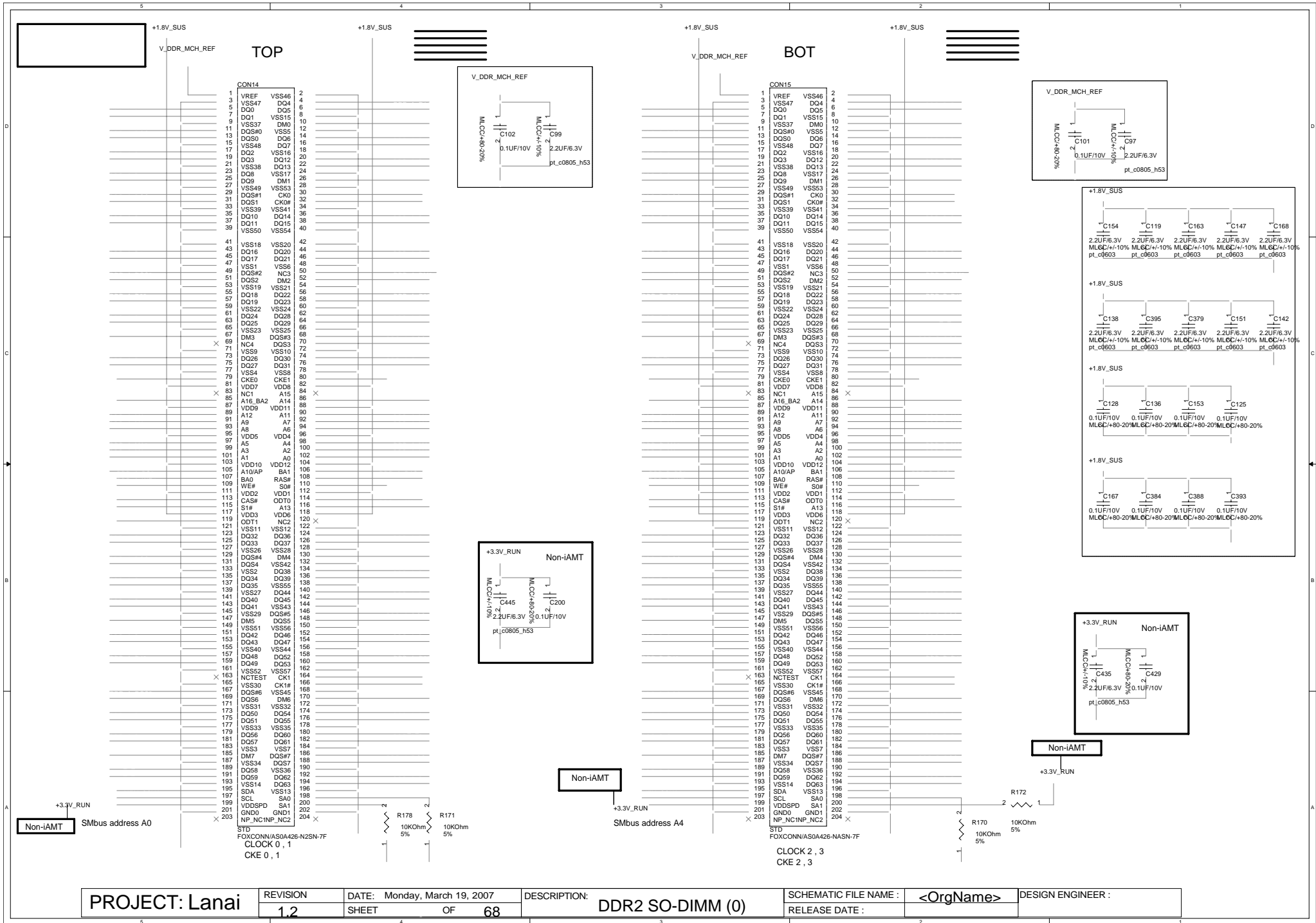


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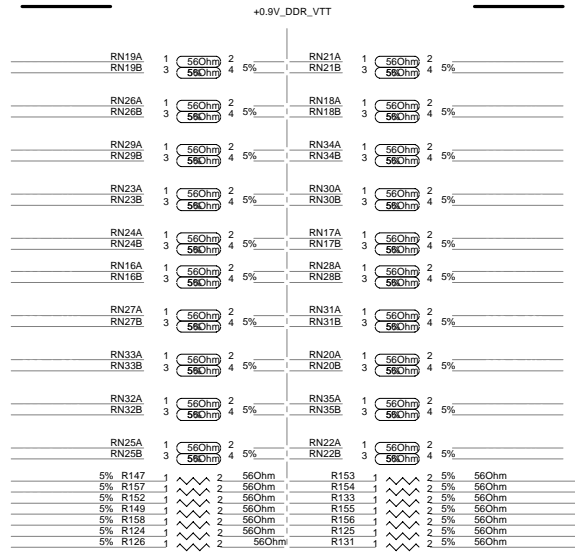
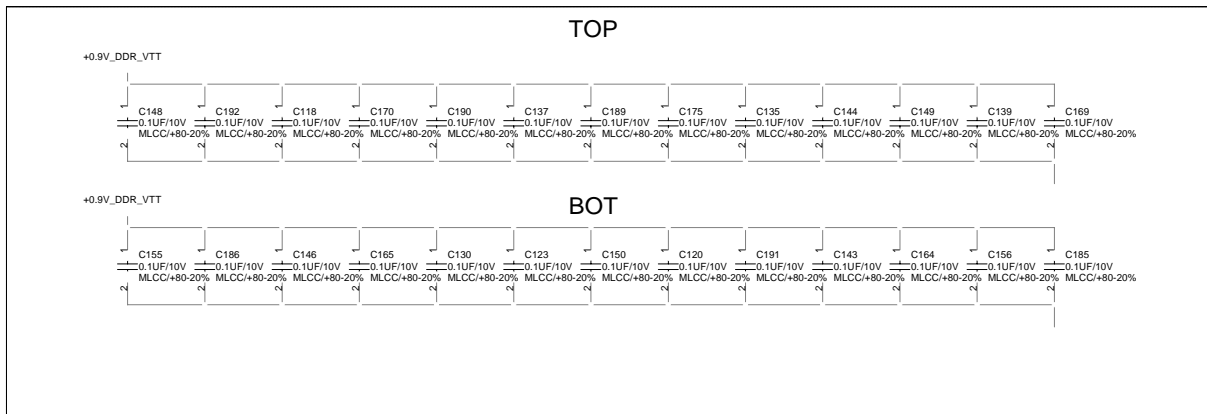


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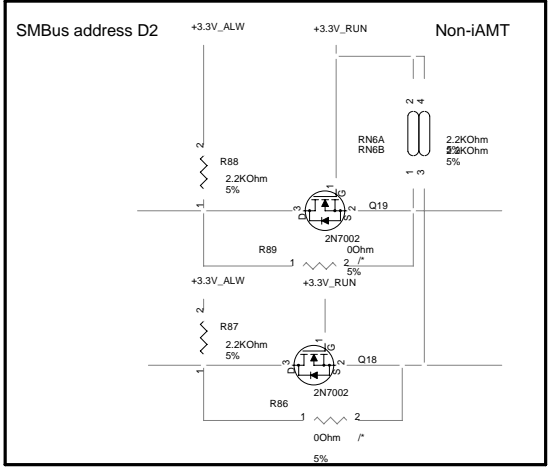
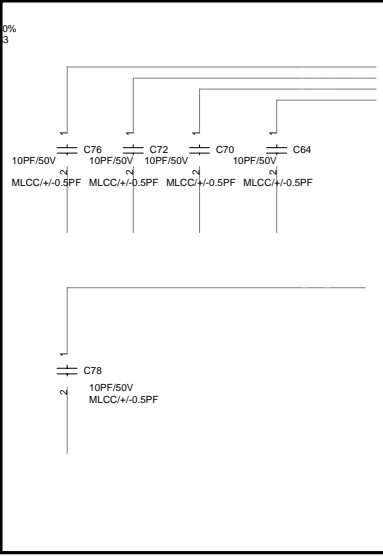
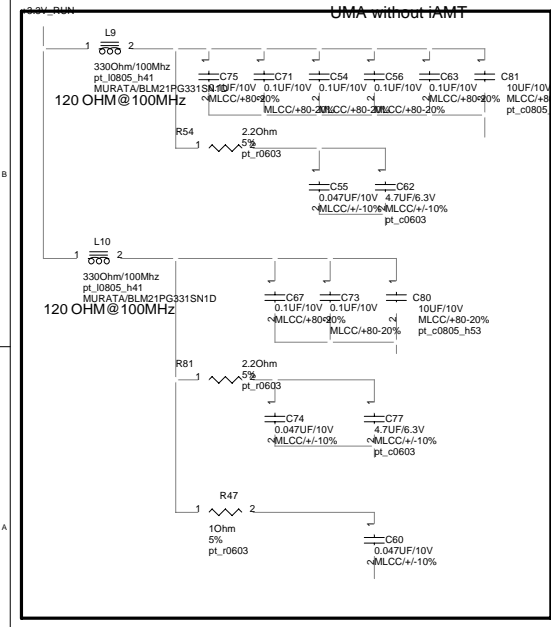
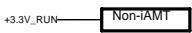
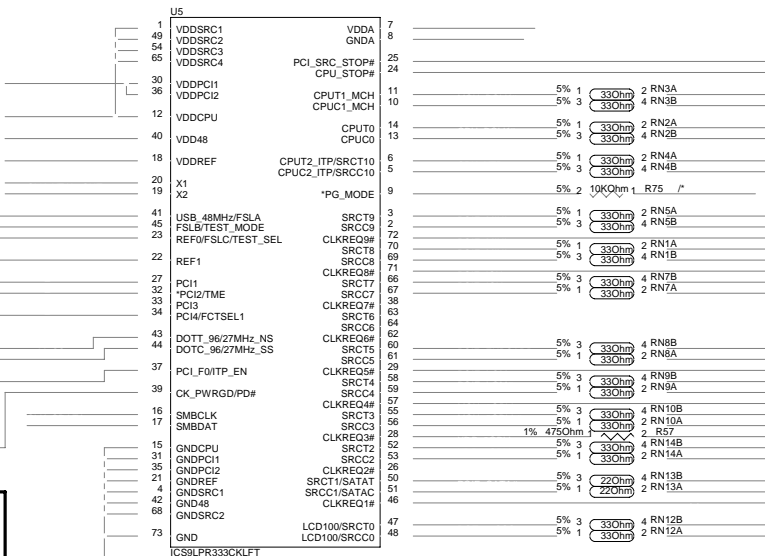
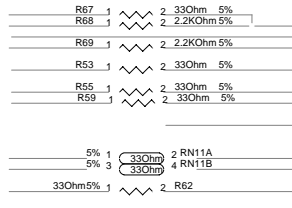
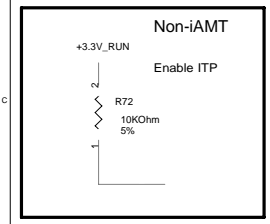
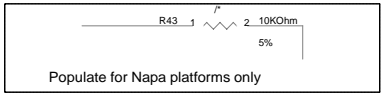
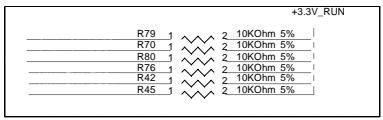
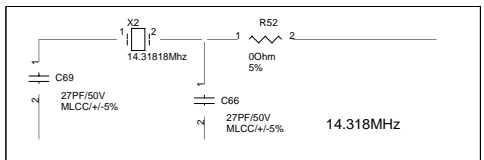
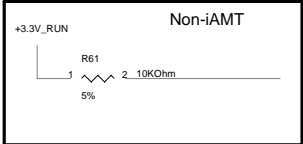
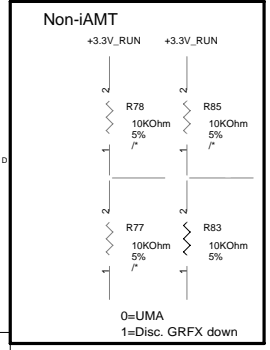


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PROJECT: Lanai	REVISION: 1.2	DATE: Monday, March 19, 2007	DESCRIPTION: DDR2 SO-DIMM (0)	SCHEMATIC FILE NAME: <OrgName>	DESIGN ENGINEER:
		SHEET OF 68		RELEASE DATE:	



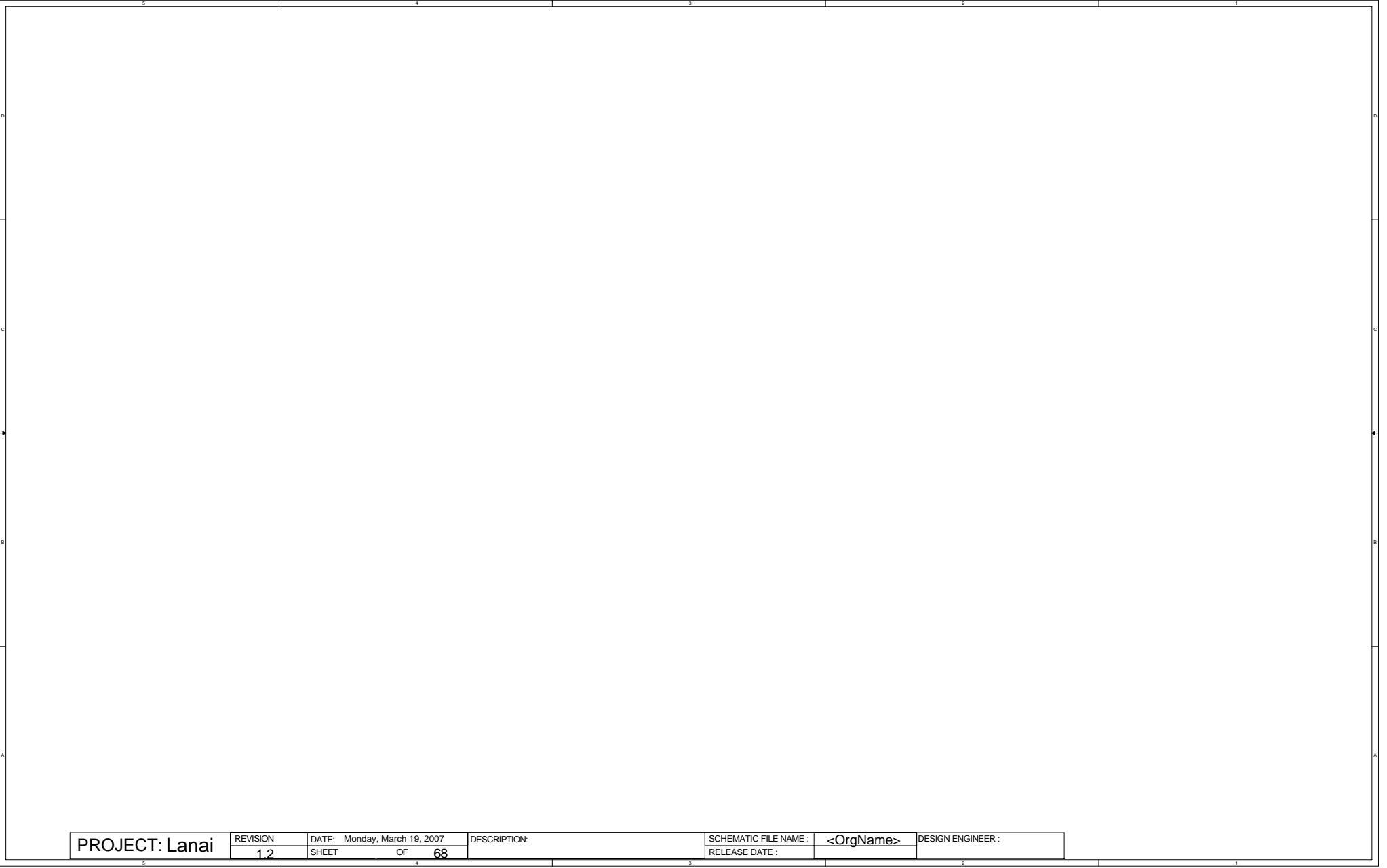
PROJECT: Lanai	REVISION	DATE: Monday, March 19, 2007	DESCRIPTION:	SCHEMATIC FILE NAME :	DESIGN ENGINEER :
	1.2	SHEET OF 68	DDR2 SO-DIMM (1)	<OrgName>	
				RELEASE DATE :	



FSC	FSB	FSA	CPU	SRC	PCI
1	0	1	100	100	33
0	0	1	133	100	33
0	1	1	166	100	33
0	1	0	200	100	33
0	0	0	266	100	33
1	0	0	333	100	33
1	1	0	400	100	33
1	1	1	RSVD	100	33

PCI_LOM=FCTSEL1

FCTSEL1(PIN 34)	Pin43	Pin44	Pin47	Pin48
0 = UMA	DOT#96T	DOT#96C	96/100M	T 96/100M_C
1 = Disc.	27Mout	27M_S\$out	SRC10	SRC10
GRFX down				



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DESCRIPTION:

SCHEMATIC FILE NAME :	<OrgName>
RELEASE DATE :	

DESIGN ENGINEER :



PROJECT: Lanai

REVISION
1.2

DATE: Monday, March 19, 2007
SHEET OF 68

DESCRIPTION:

SCHEMATIC FILE NAME : <OrgName>
RELEASE DATE :

DESIGN ENGINEER :

1				1
2				2
3				3
4				4
5				5

PROJECT: Lanai

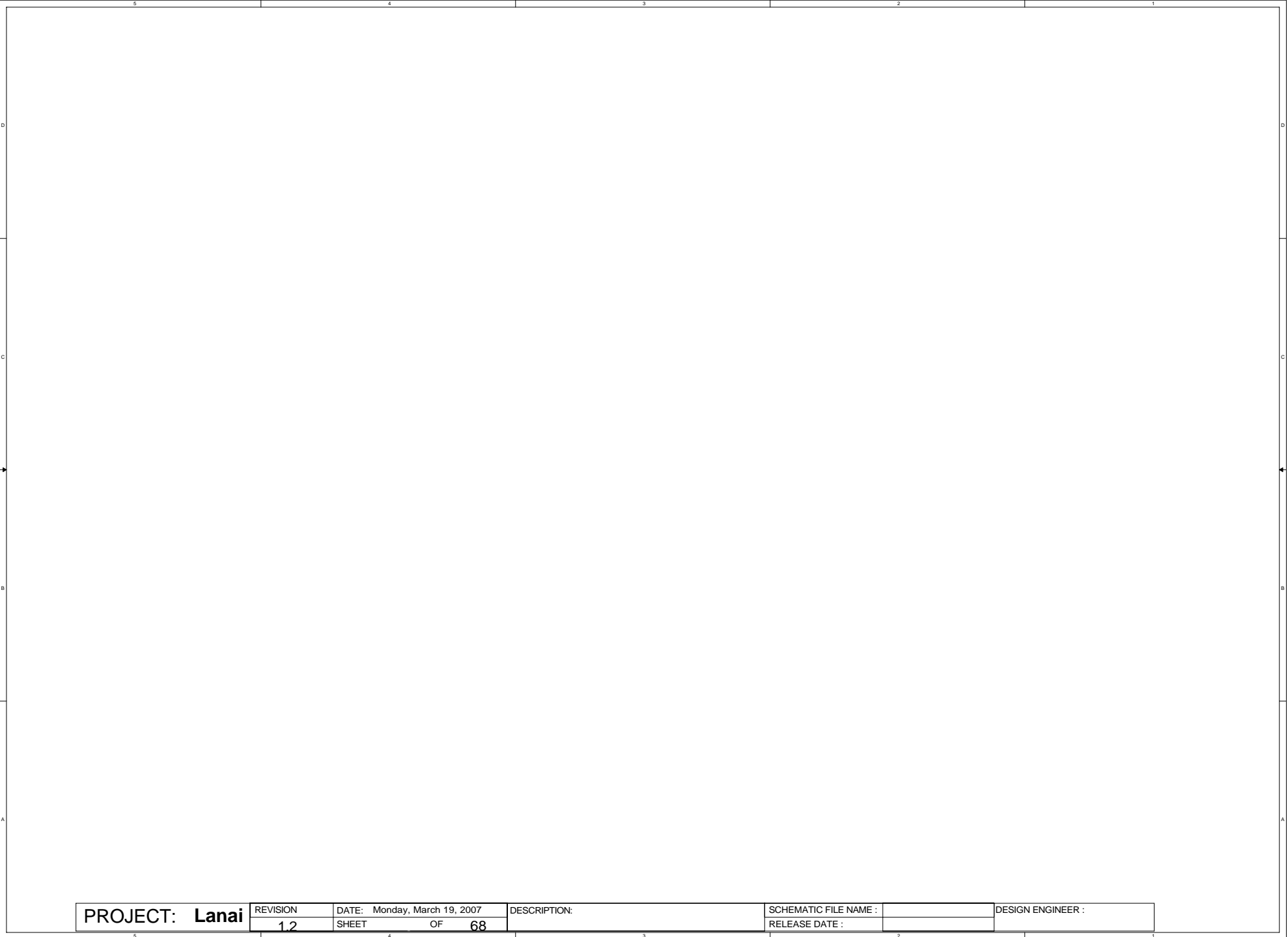
REVISION
1.2

DATE: Monday, March 19, 2007
SHEET OF **68**

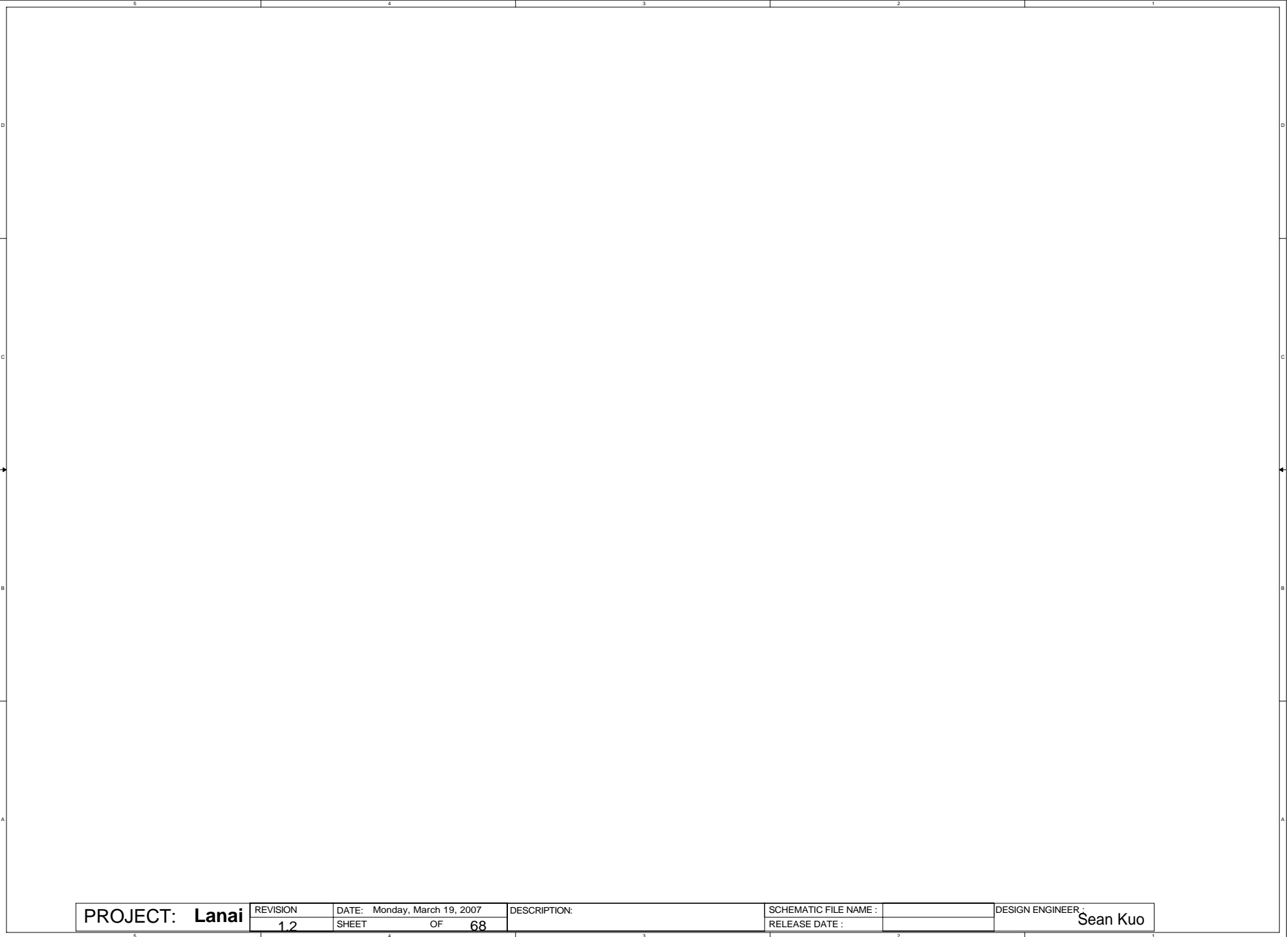
DESCRIPTION:

SCHEMATIC FILE NAME : **<OrgName>**
RELEASE DATE :

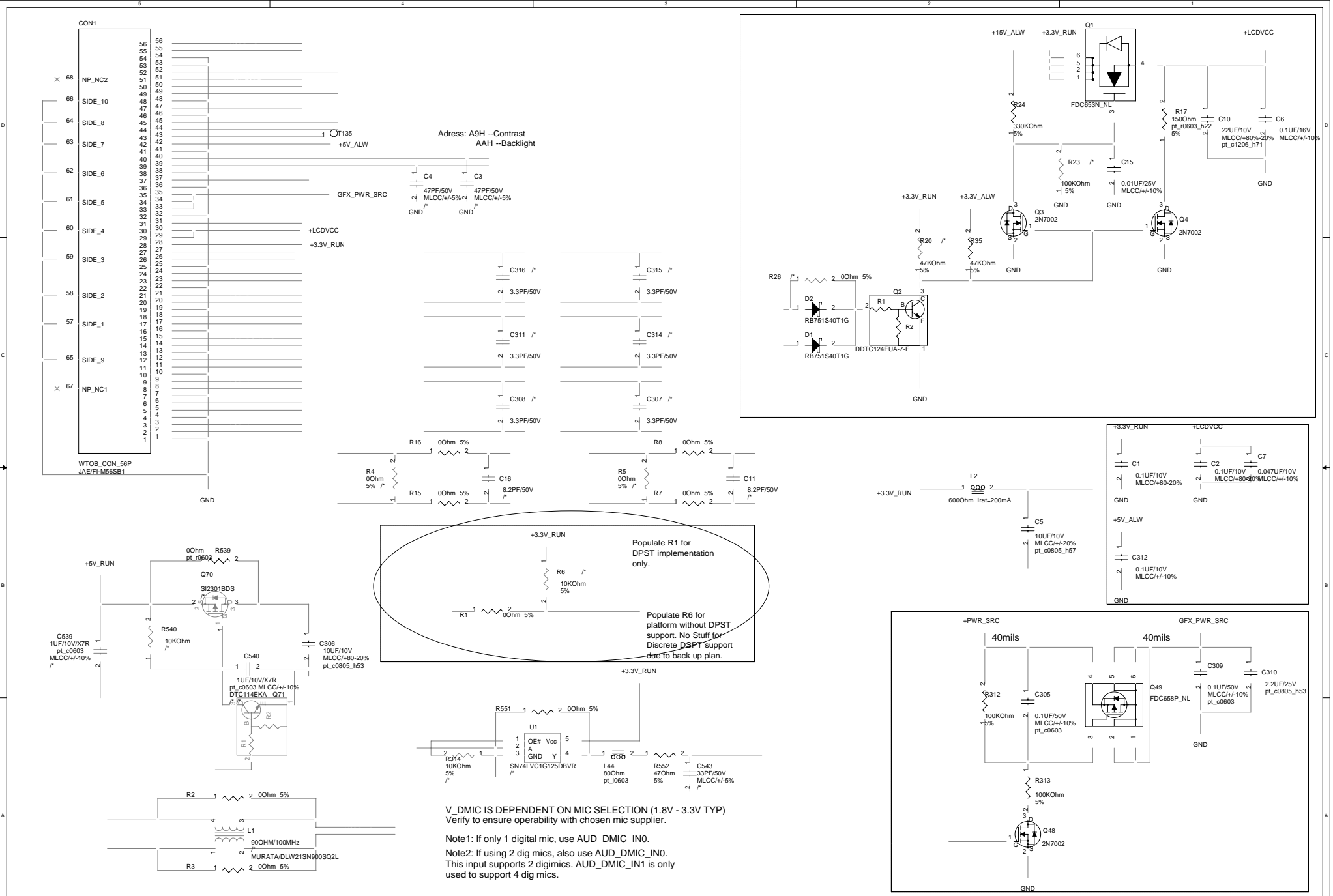
DESIGN ENGINEER :



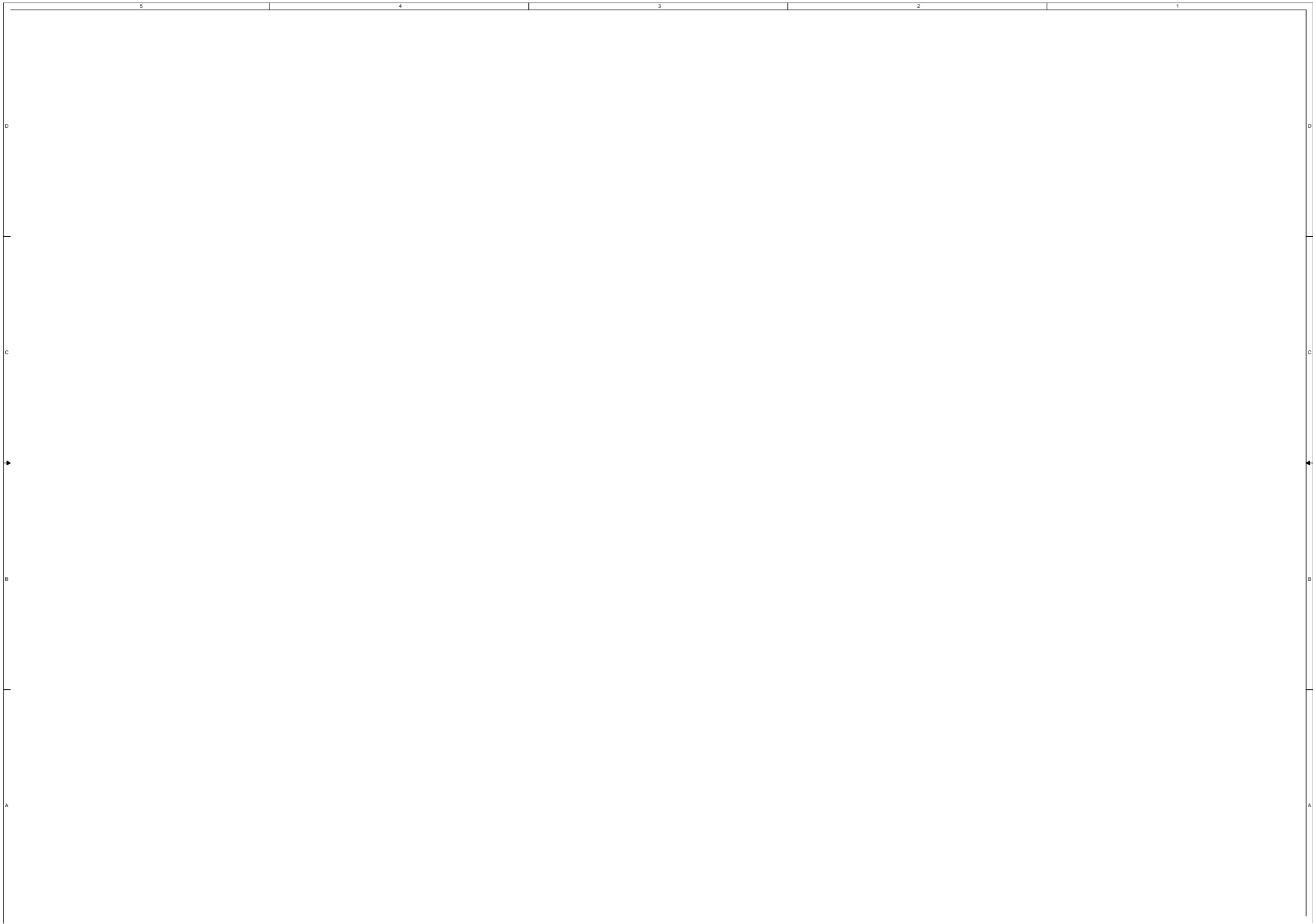
PROJECT: Lanai	REVISION	DATE: Monday, March 19, 2007	DESCRIPTION:	SCHMATIC FILE NAME :	DESIGN ENGINEER :
	1.2	SHEET OF 68		RELEASE DATE :	

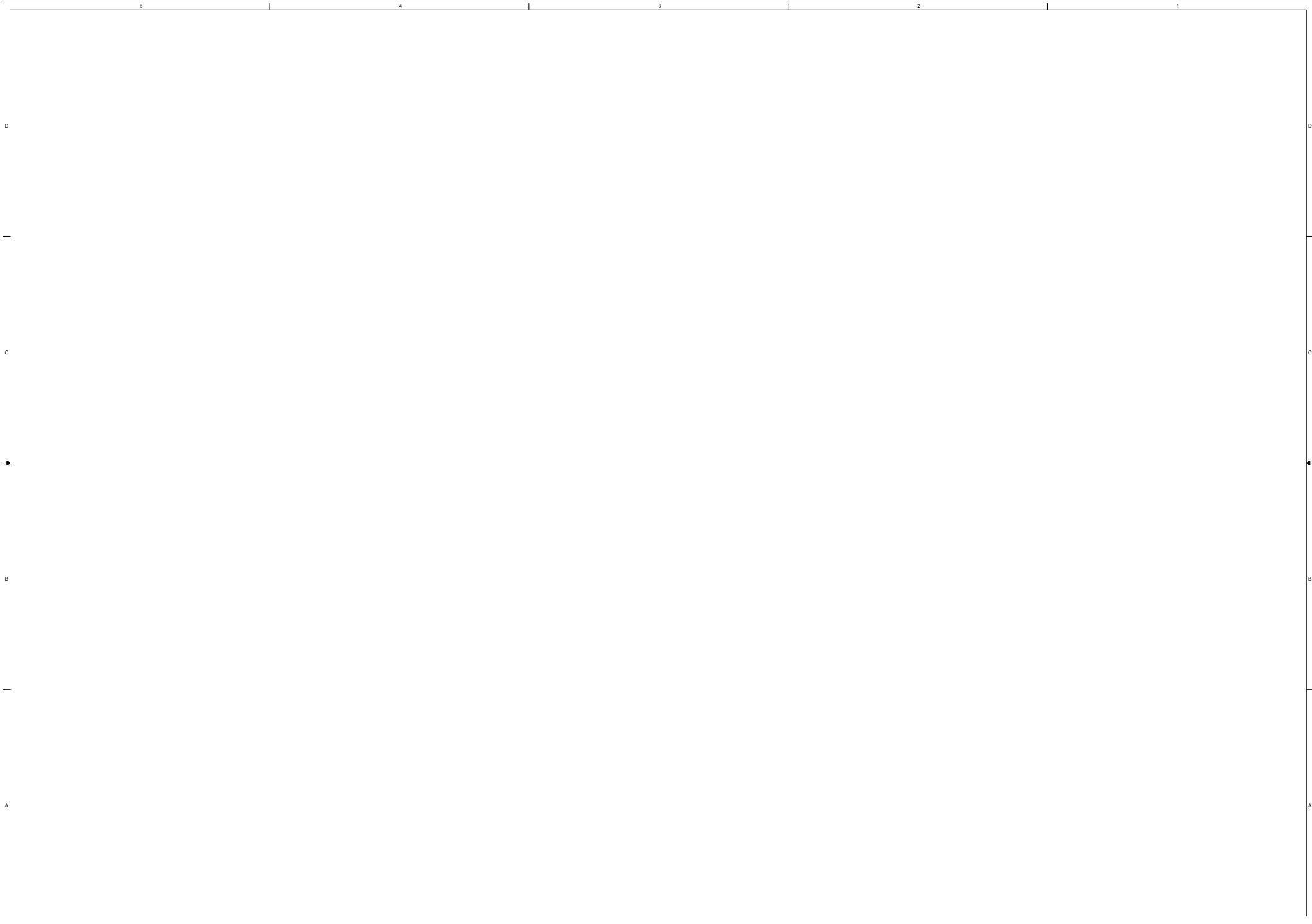


PROJECT: Lanai	REVISION	DATE: Monday, March 19, 2007	DESCRIPTION:	SCHMATIC FILE NAME :	DESIGN ENGINEER
	1.2	SHEET OF 68		RELEASE DATE :	Sean Kuo

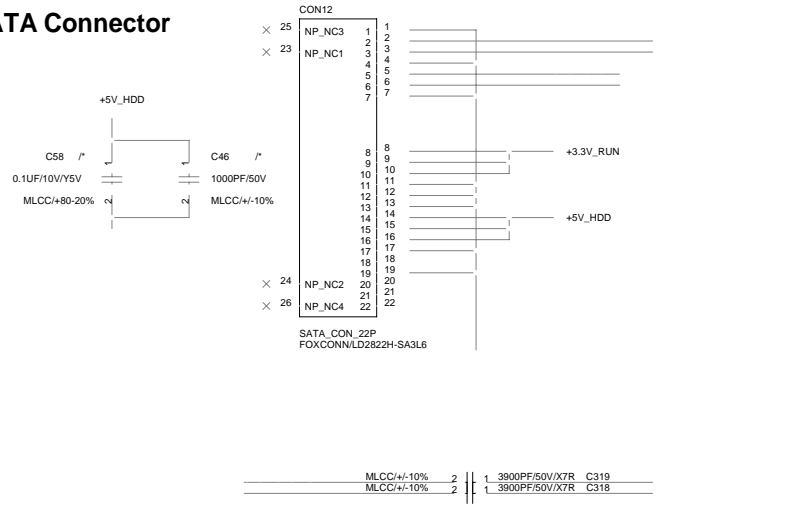


PROJECT: Lanai	REVISION: 1.2	DATE: Monday, March 19, 2007	DESCRIPTION: LVDS CON	SCHEMATIC FILE NAME:	DESIGN ENGINEER:
		SHEET OF 68		RELEASE DATE:	

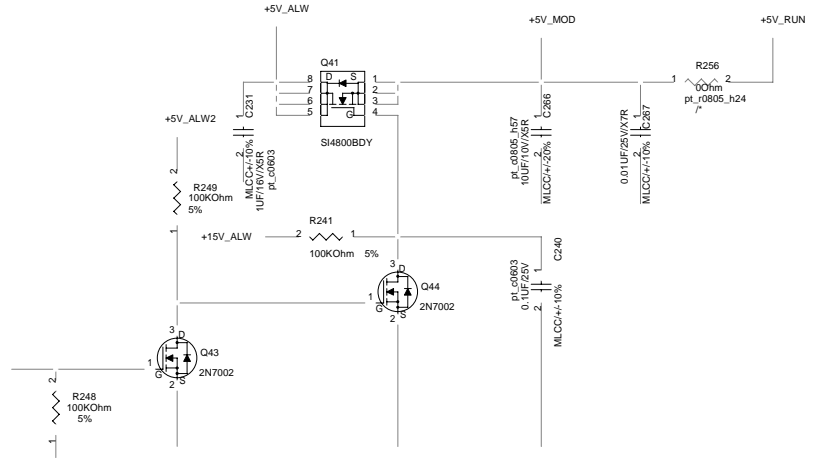
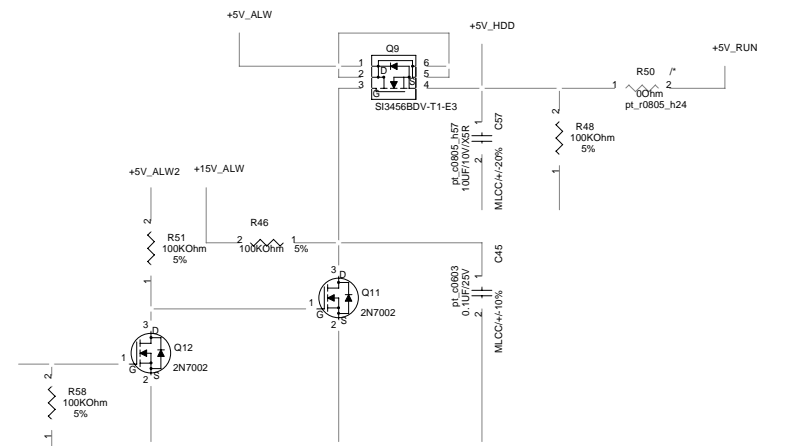
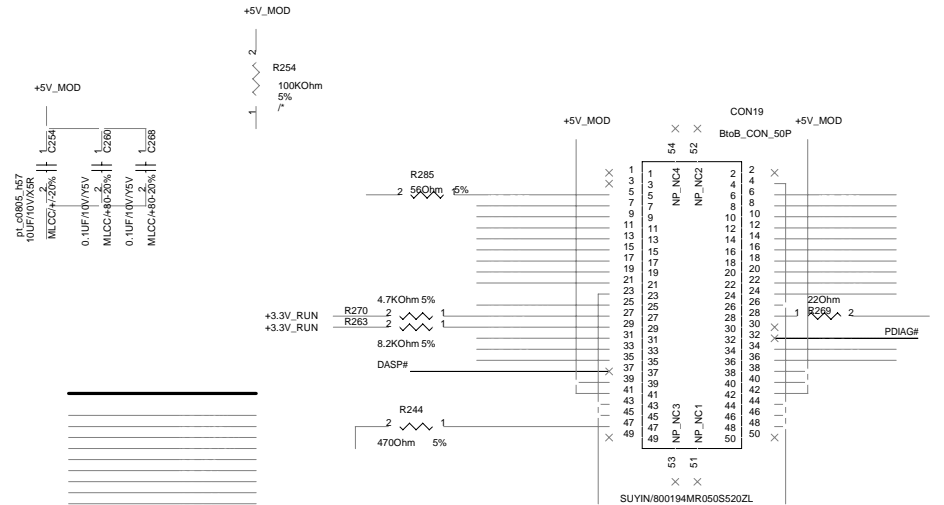




SATA Connector



ODD Connector

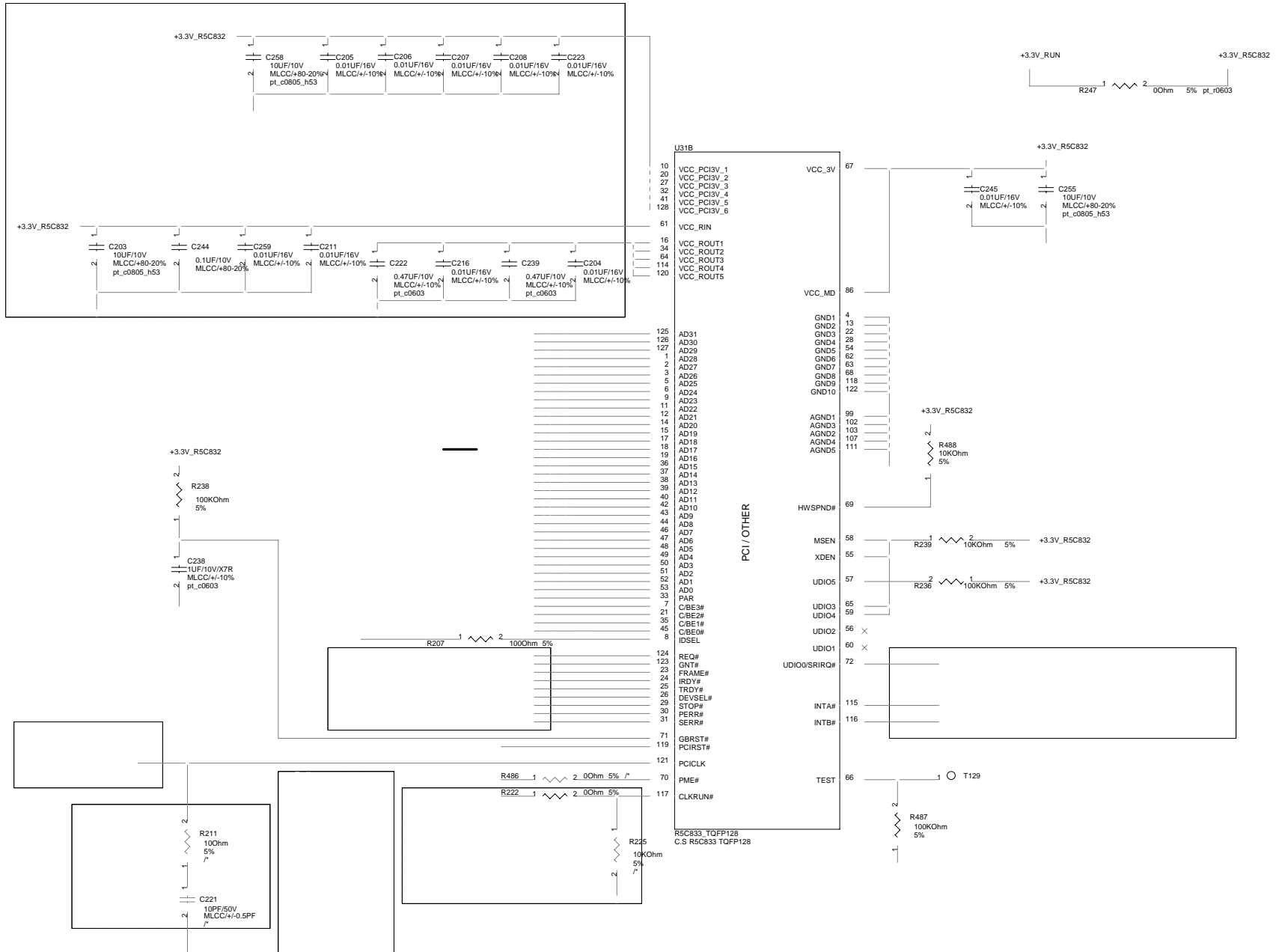


PROJECT: Lanai

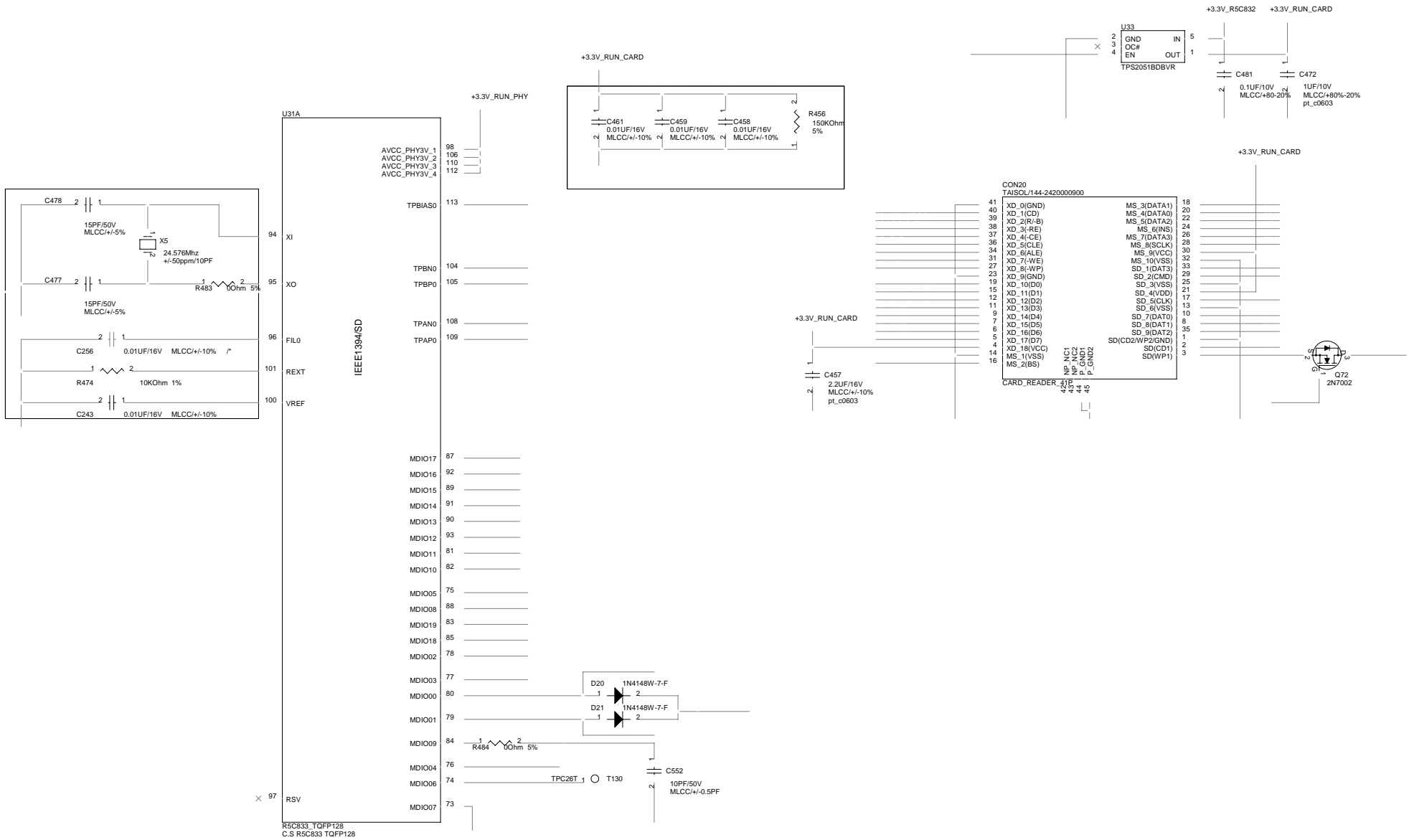
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DESCRIPTION: SATA(HDD & CD_ROM)

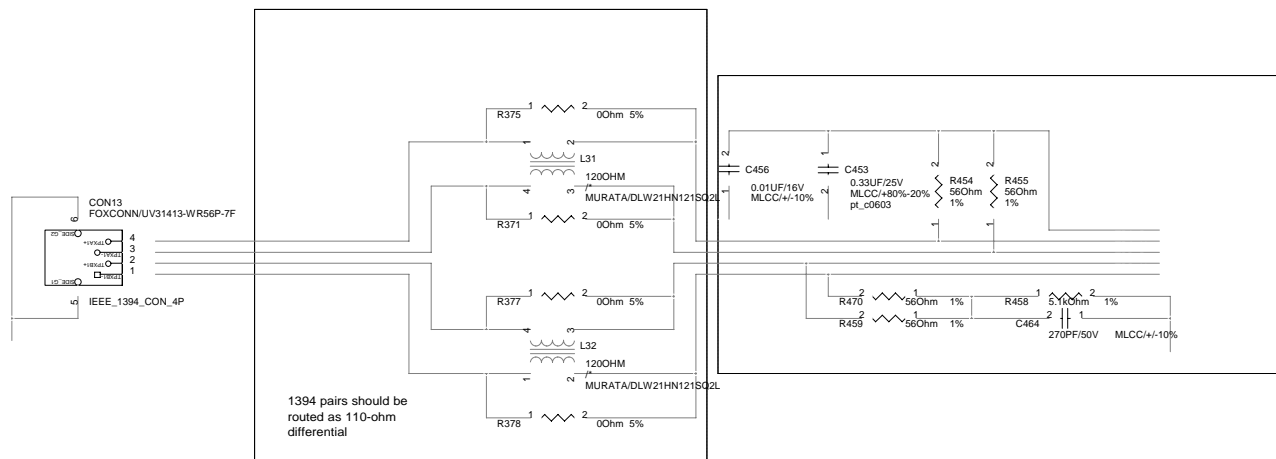
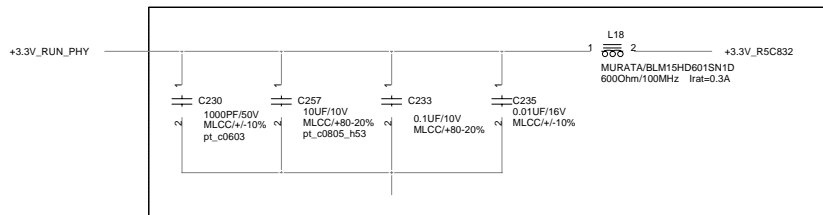
SCHEMATIC FILE NAME: <OrgName>
 RELEASE DATE:
 DESIGN ENGINEER:



PROJECT: Lanai	REVISION	DATE: Monday, March 19, 2007	DESCRIPTION:	SCHEMATIC FILE NAME :	<OrgName>	DESIGN ENGINEER :
	1.2	SHEET OF 68	R5C833 - PCI INTERFACE	RELEASE DATE :		

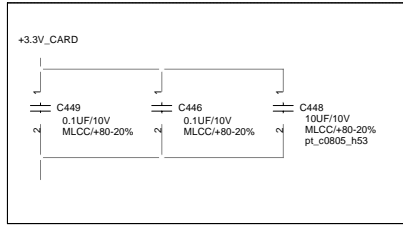
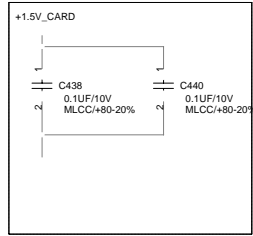
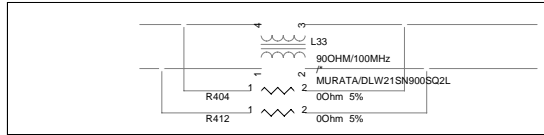


PROJECT: Lanai	REVISION	DATE: Monday, March 19, 2007	DESCRIPTION:	SCHEMATIC FILE NAME :	<OrgName>	DESIGN ENGINEER :
	1.2	SHEET OF 68	R5C833 - FLASH MEMORY PART	RELEASE DATE :		

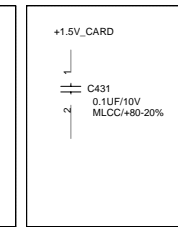
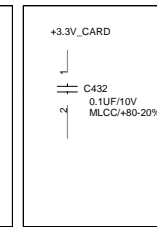
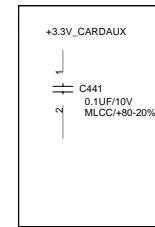
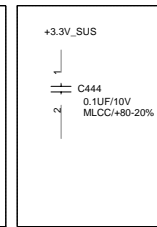
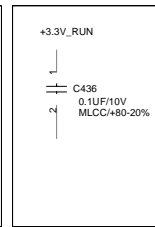
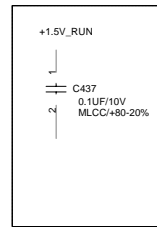
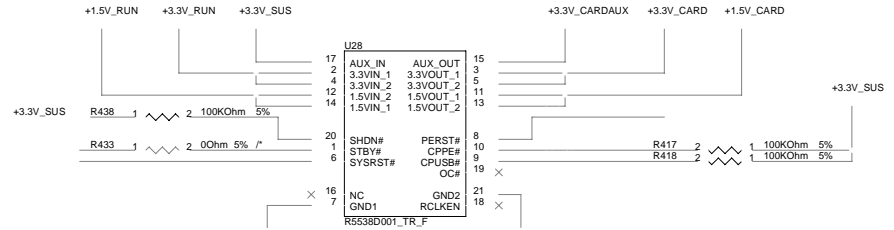
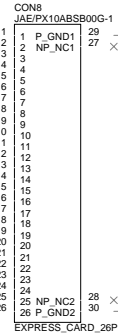


PROJECT: Lanai	REVISION	DATE: Monday, March 19, 2007	DESCRIPTION:	SCHEMATIC FILE NAME :	<OrgName>	DESIGN ENGINEER :
	1.2	SHEET OF 68	R5C833 - IEEE1394 PART	RELEASE DATE :		

Express Card



+1.5V_CARD
+3.3V_CARDAUX
+3.3V_CARD



PROJECT: Lanai

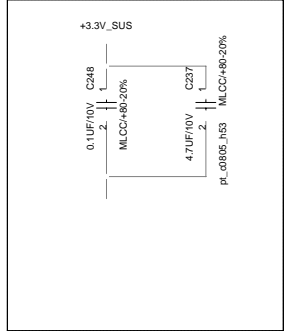
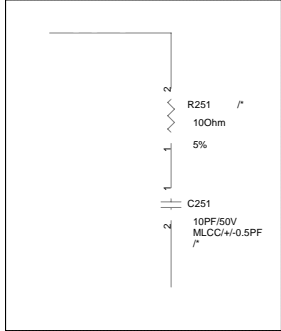
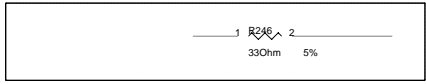
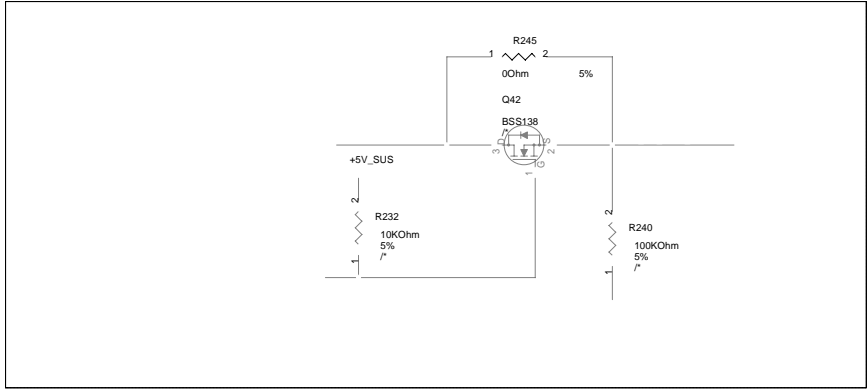
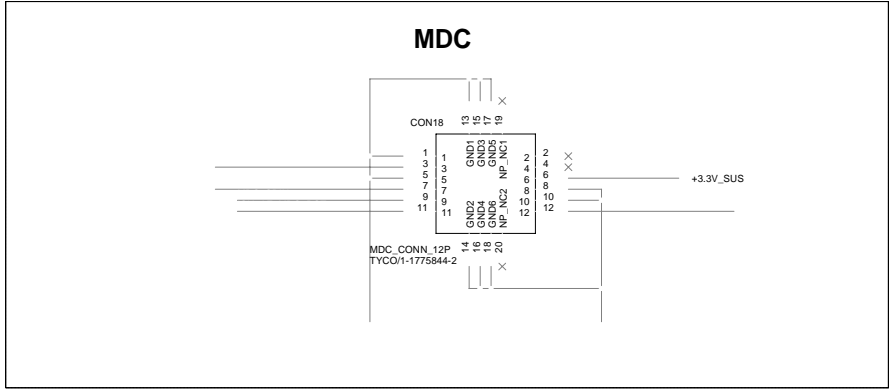
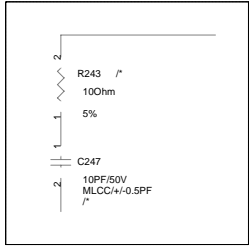
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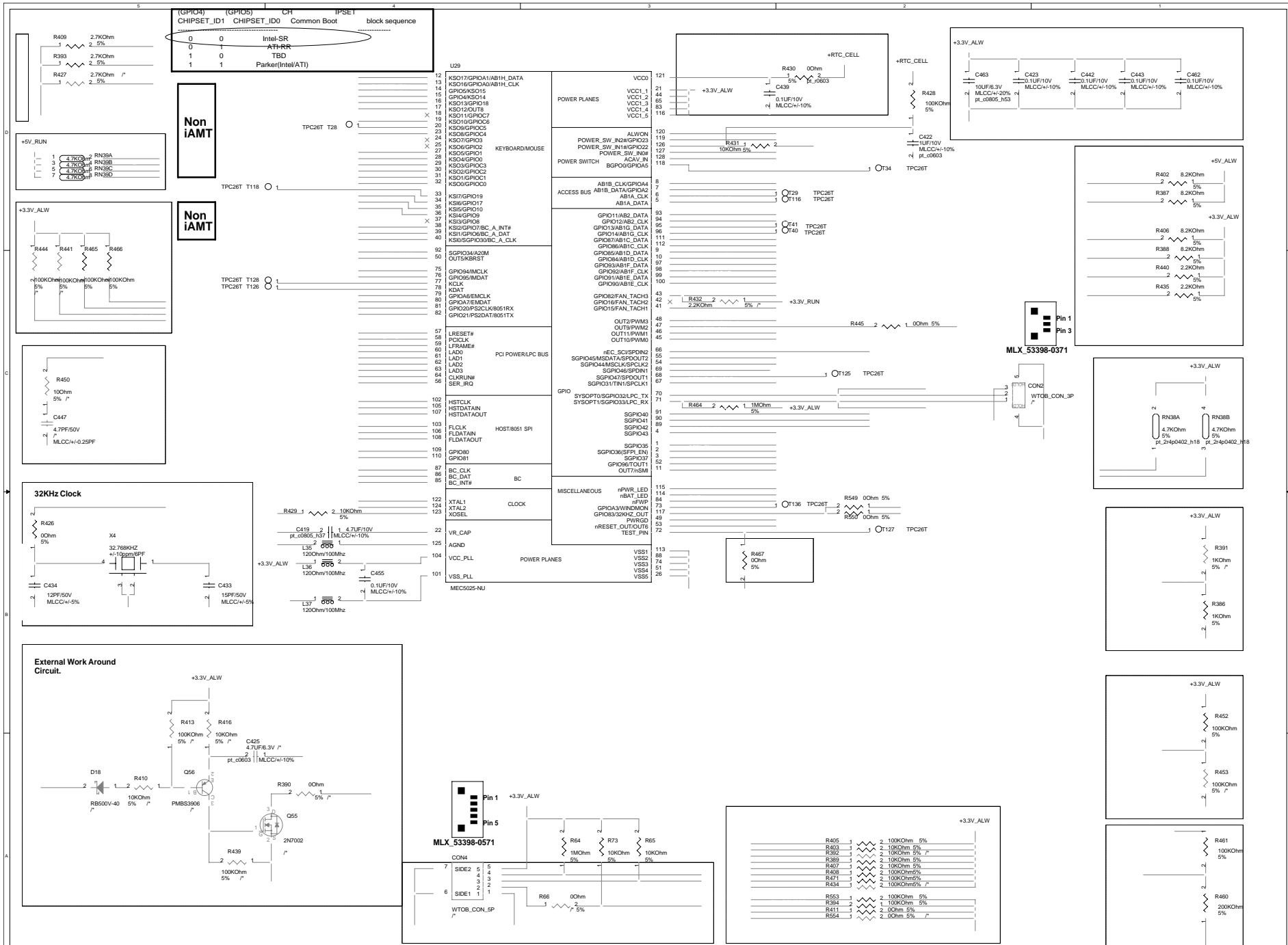
DESCRIPTION:
PCI-Express Card

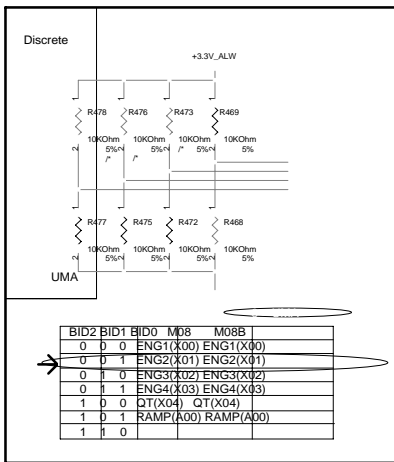
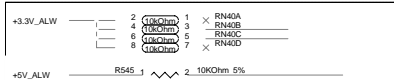
SCHEMATIC FILE NAME : <OrgName>
RELEASE DATE :

DESIGN ENGINEER :
Terry Lin

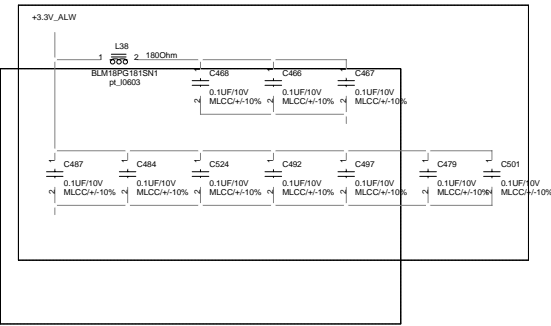
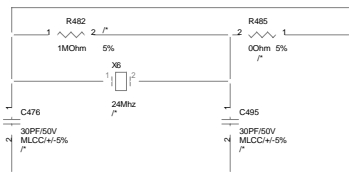


PROJECT: Lanai	REVISION	DATE: Monday, March 19, 2007	DESCRIPTION:	SCHMATIC FILE NAME :	DESIGN ENGINEER :
	1.2	SHEET OF 68	MDC_CONN	<OrgName>	
				RELEASE DATE :	





24MHz Clock



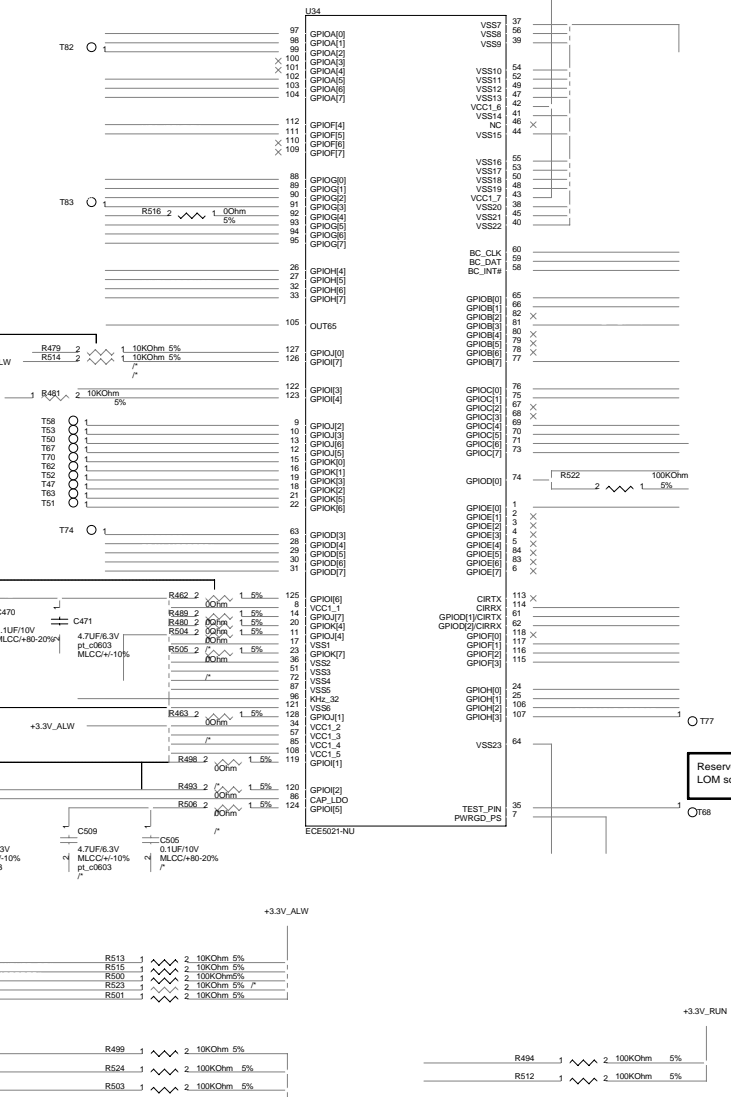
R514 R479, ECE5011 is suff, ECE5021 is not stuff

Note: for ECE5011 only ECE5021 will be non_ stuff

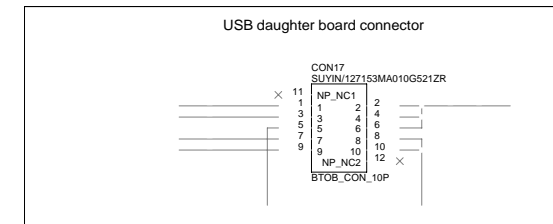
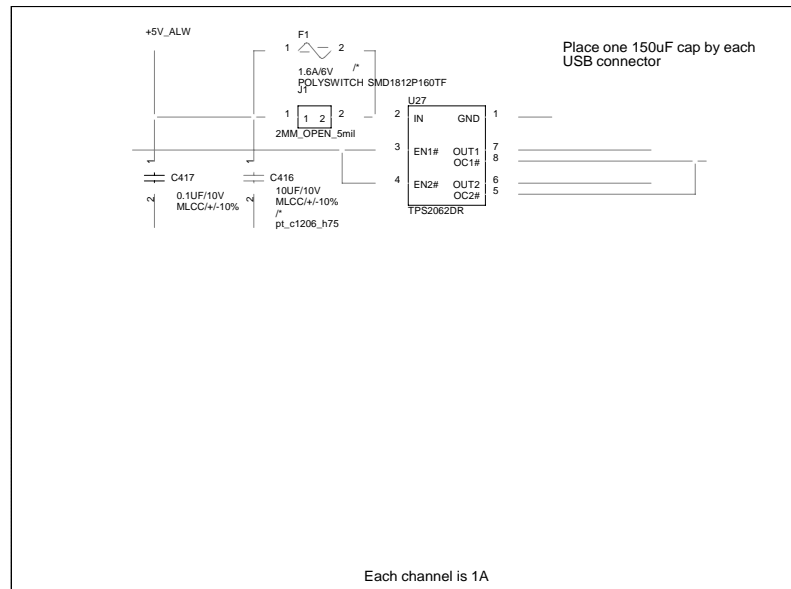
R462 R489 R480, ECE 5011 is suff, ECE5021 is not stuff

R504 R505 R463, EC E5011 is suff, ECE5021 is not stuff

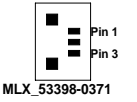
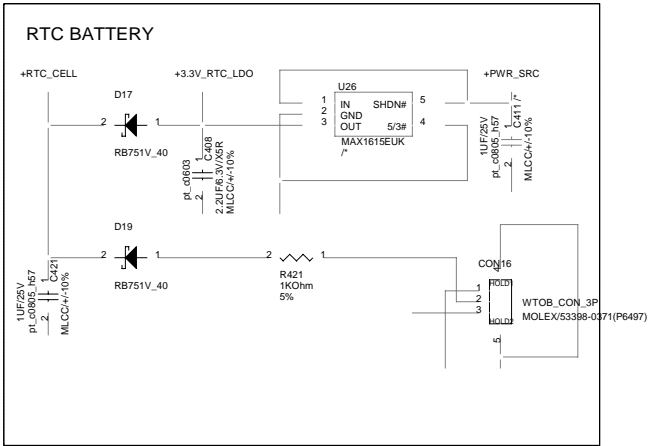
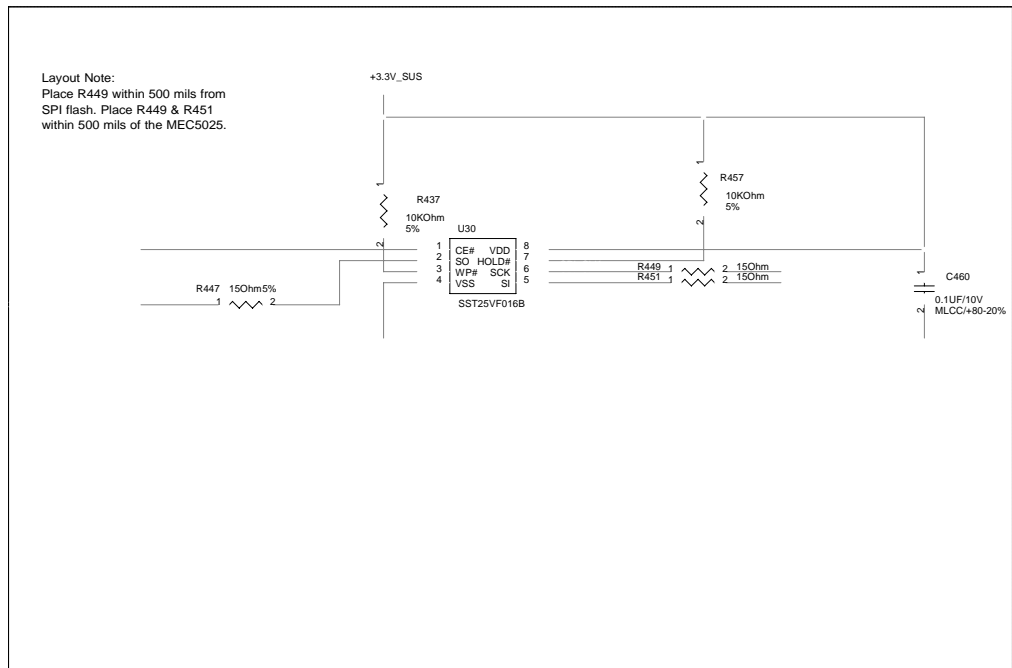
R498 R493 R506, EC E5011 is suff, ECE5021 is not stuff



Reserved for Broadcom LOM solution

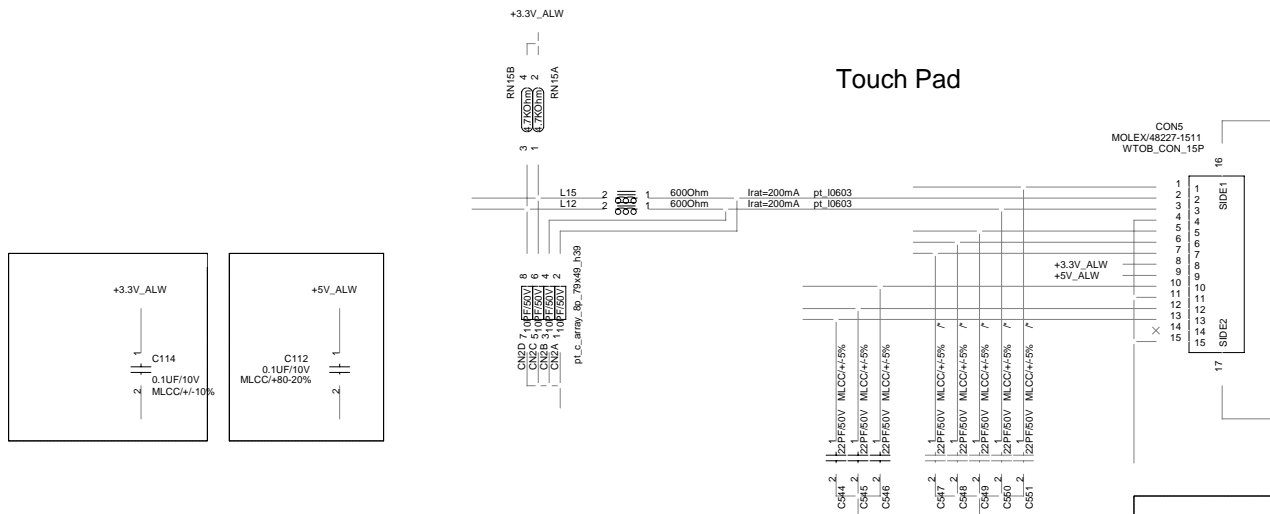


PROJECT: Lanai	REVISION	DATE: Monday, March 19, 2007	DESCRIPTION:	SCHMATIC FILE NAME :	<OrgName>	DESIGN ENGINEER :
	1.2	SHEET OF 68	USB PORT x 2	RELEASE DATE :		Terry Lin

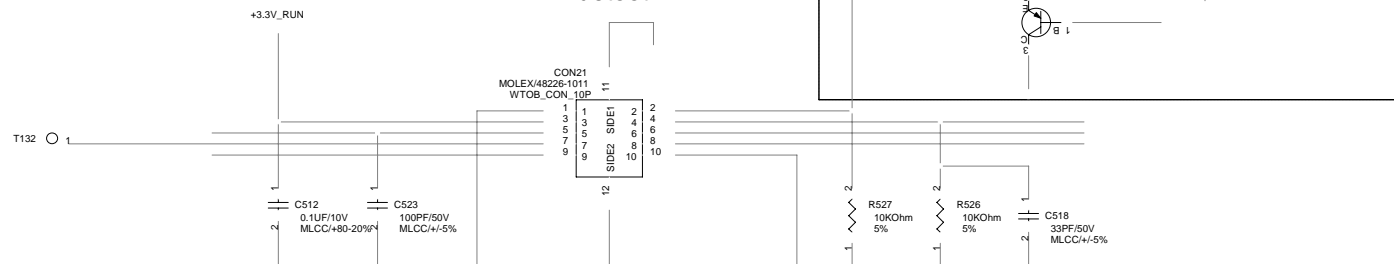


PROJECT: Lanai	REVISION	DATE: Monday, March 19, 2007	DESCRIPTION:	SCHMATIC FILE NAME :	DESIGN ENGINEER :
	1.2	SHEET OF 68	FLASH & RTC	<OrgName>	C.L. Ho
RELEASE DATE :					

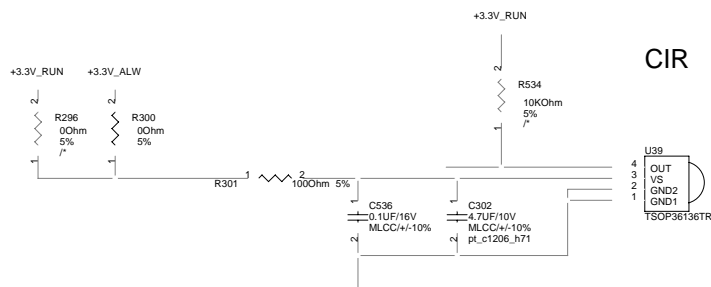
Touch Pad



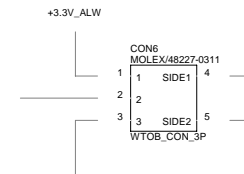
Bluetooth



CIR



HALL SENSOR



PROJECT: Lanai

REVISION
1.2

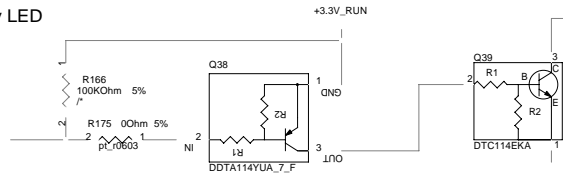
DATE: Monday, March 19, 2007
SHEET OF 68

DESCRIPTION:
TOUCH PAD & BT & CIR & LID

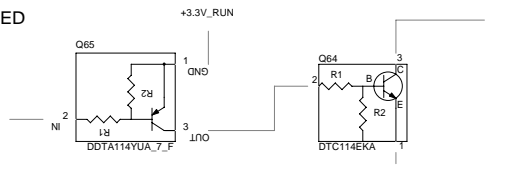
SCHEMATIC FILE NAME: <OrgName>

DESIGN ENGINEER :

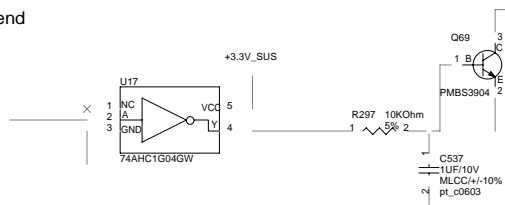
HDD activity LED



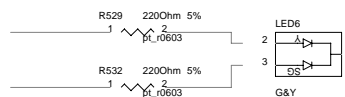
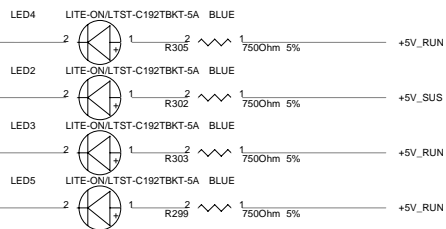
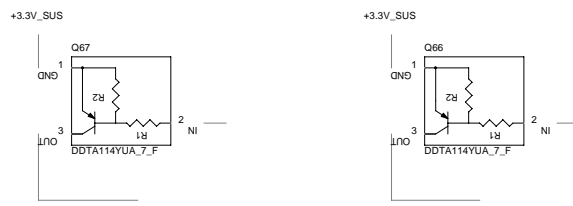
BT activity LED



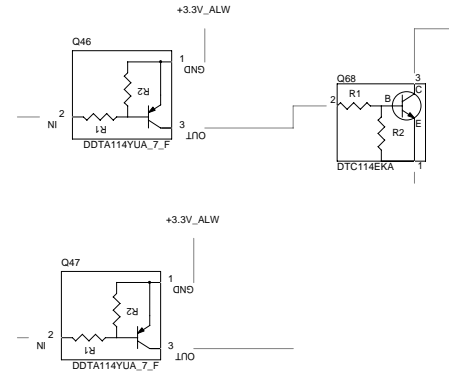
Power&Suspend



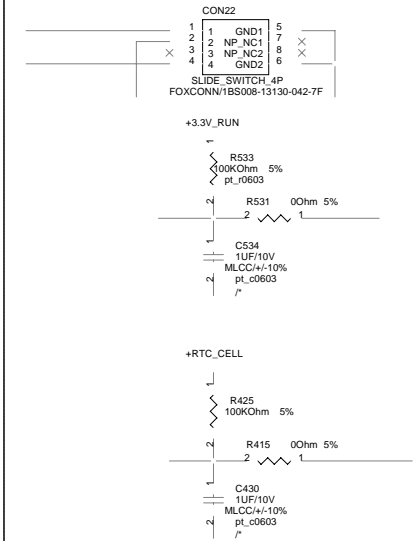
Sniffer LED driver circuit



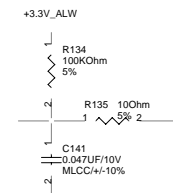
Battery status



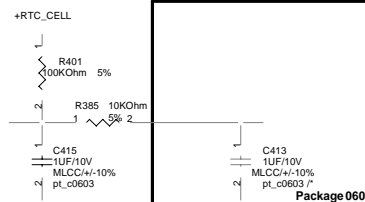
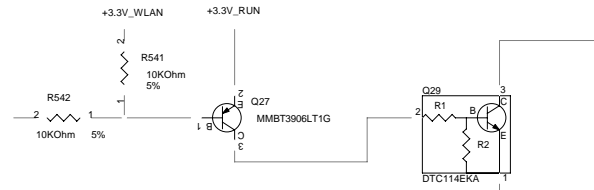
Sniffer Switch



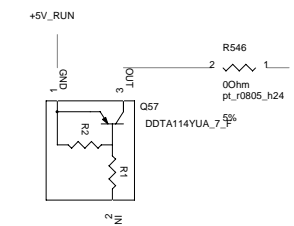
Hall Switch



WLAN



Media Bottom Board LED drive circuit



PROJECT: Lanai

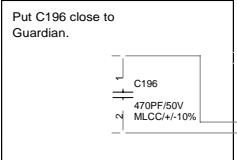
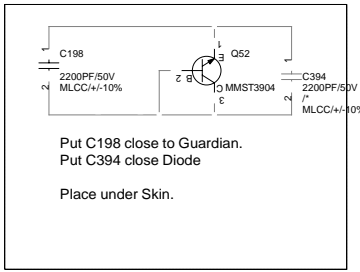
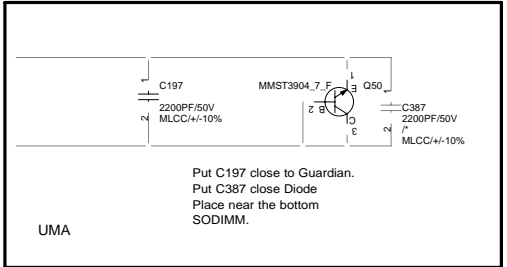
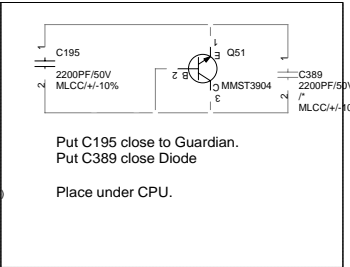
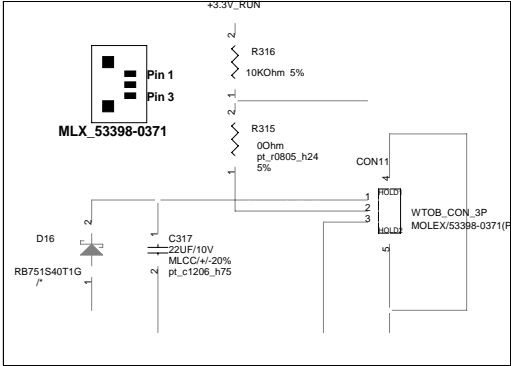
REVISION
1.2

DATE: Monday, March 19, 2007
SHEET OF 68

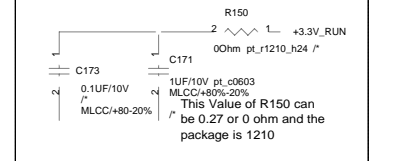
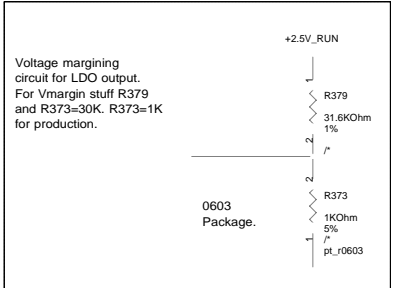
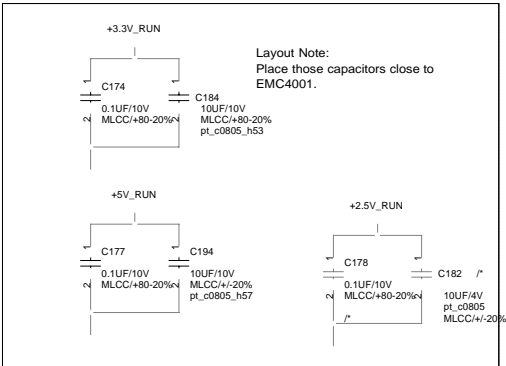
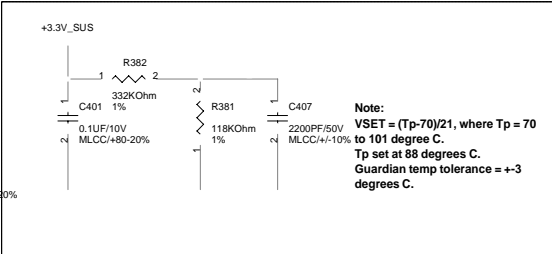
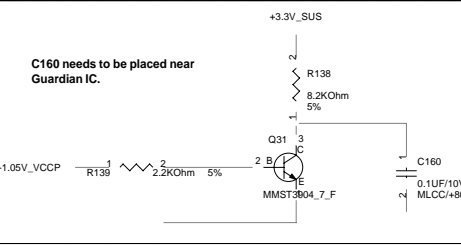
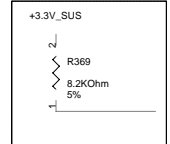
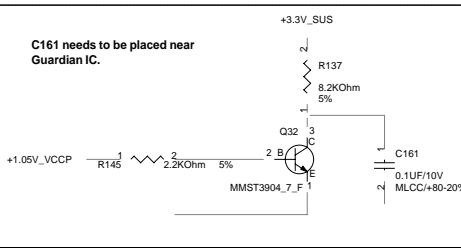
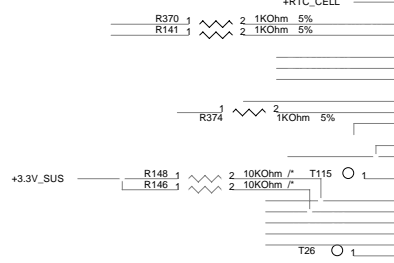
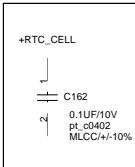
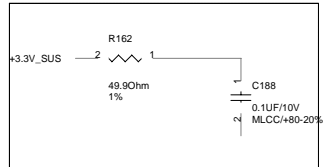
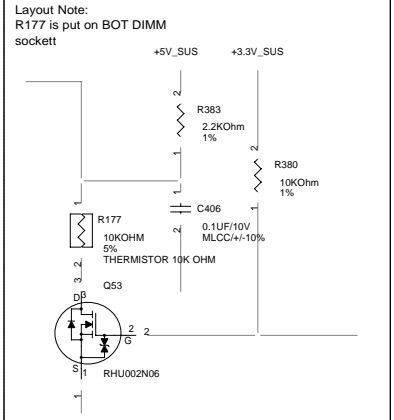
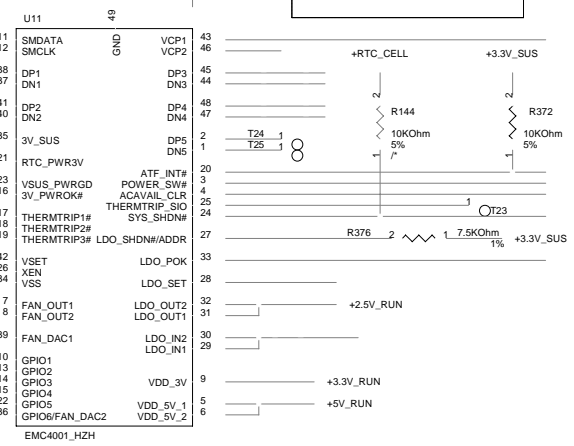
DESCRIPTION:
SWITCH & LED

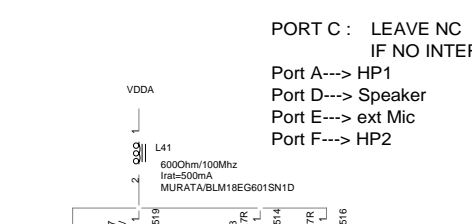
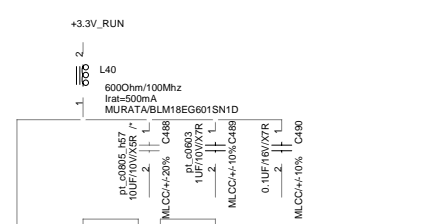
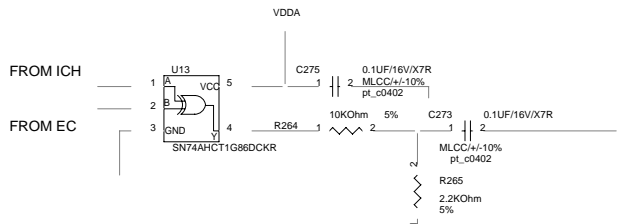
SCHEMATIC FILE NAME : <OrgName>
RELEASE DATE :

DESIGN ENGINEER :
C

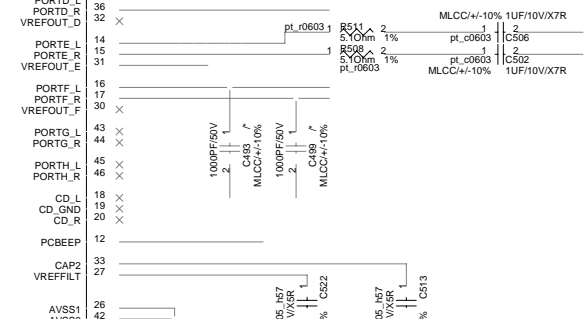
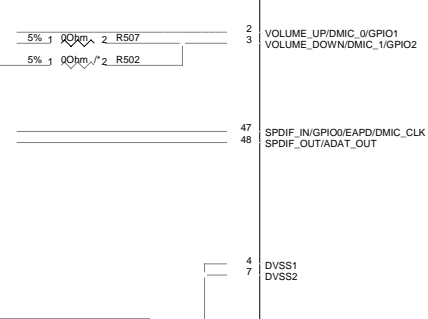
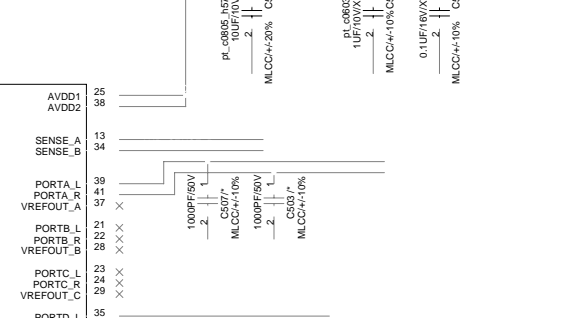
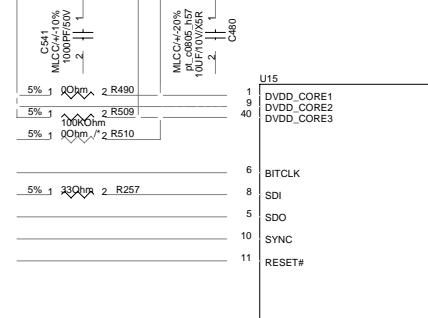


Guardian

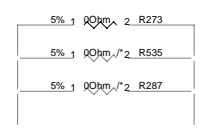
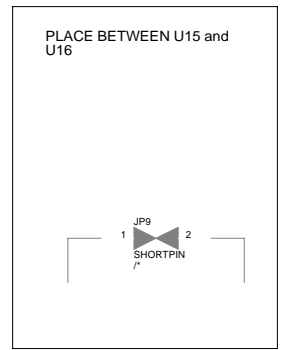
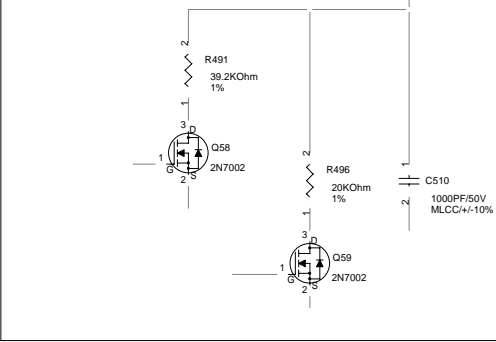
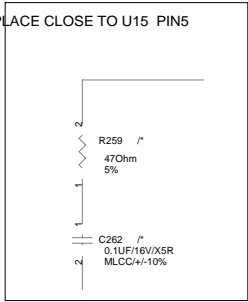
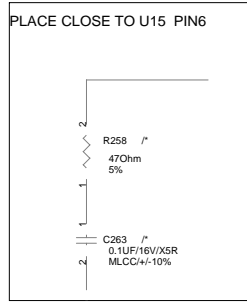
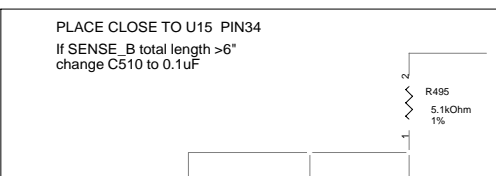
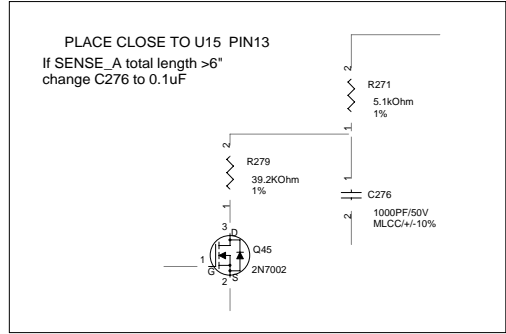




PORT C : LEAVE NC
IF NO INTERNAL MICS.
Port A--> HP1
Port D--> Speaker
Port E--> ext Mic
Port F--> HP2



For TV port



PROJECT: Lanai

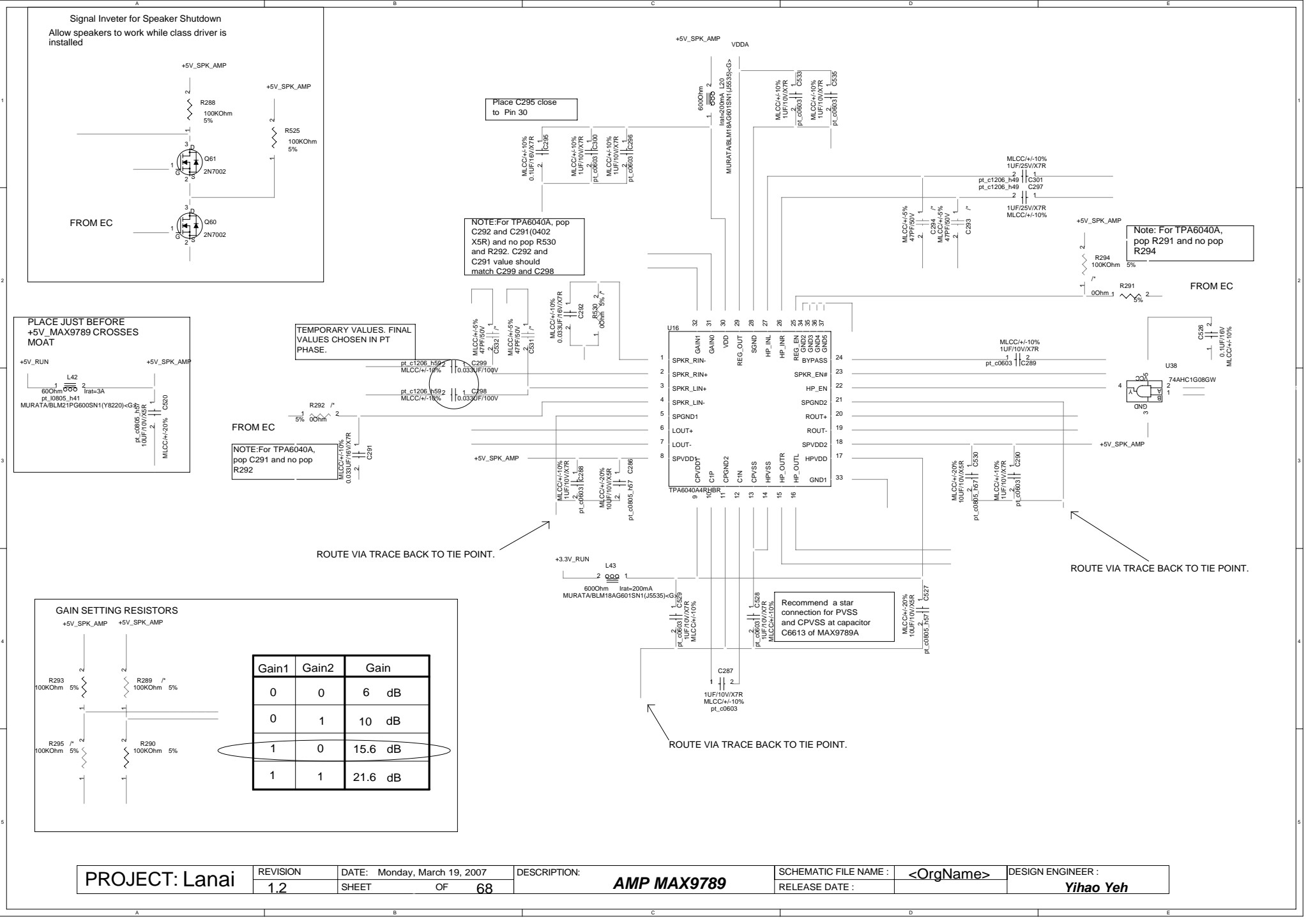
REVISION
1.2

DATE: Monday, March 19, 2007
SHEET OF 68

DESCRIPTION:
STAC9228

SCHEMATIC FILE NAME :
RELEASE DATE :

DESIGN ENGINEER :
Yihao Yeh



PLACE JUST BEFORE +5V_MAX9789 CROSSES MOAT

Components: L42 (60Ohm), pt_J0805_h41, MURATA/BLM21PG600SN1(Y8220)-G, C520, pt_c0605_h167, 10UF/10V/X7R, MLCC/H-20%

NOTE: For TPA6040A, pop C291 and no pop R292

NOTE: For TPA6040A, pop C292 and C291 (0402 X5R) and no pop R530 and R292. C292 and C291 value should match C299 and C298

TEMPORARY VALUES. FINAL VALUES CHOSEN IN PT PHASE.

Note: For TPA6040A, pop R291 and no pop R294

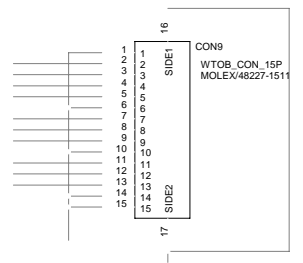
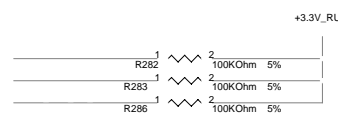
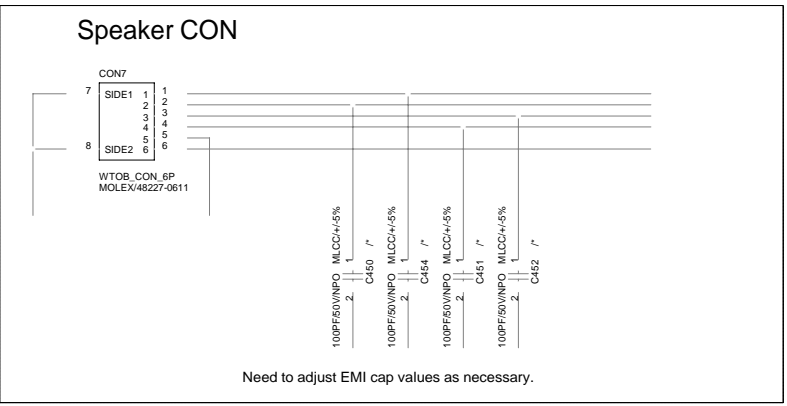
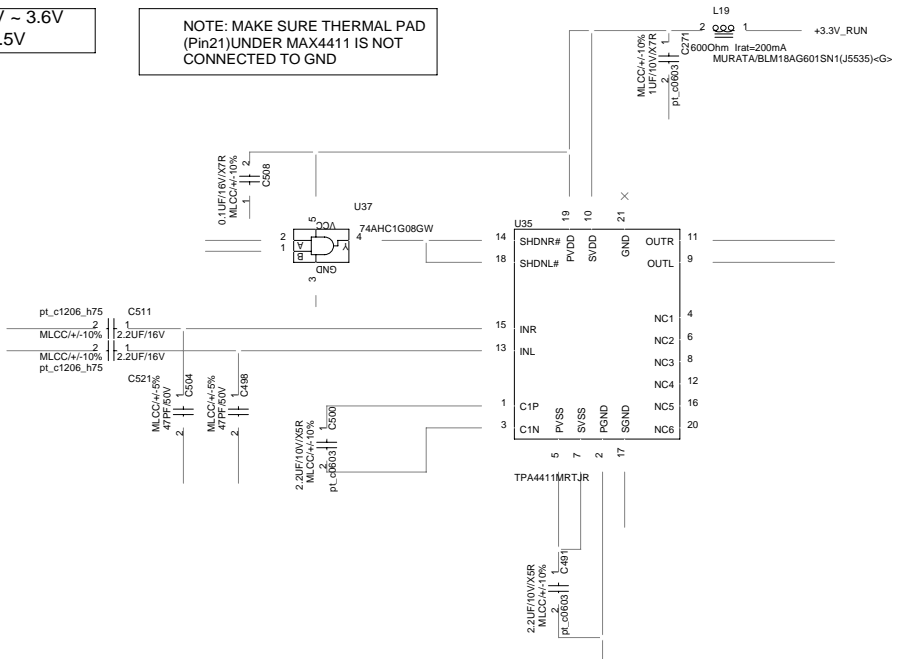
GAIN SETTING RESISTORS

Components: R293 (100KOhm 5%), R289 (100KOhm 5%), R295 (100KOhm 5%), R290 (100KOhm 5%)

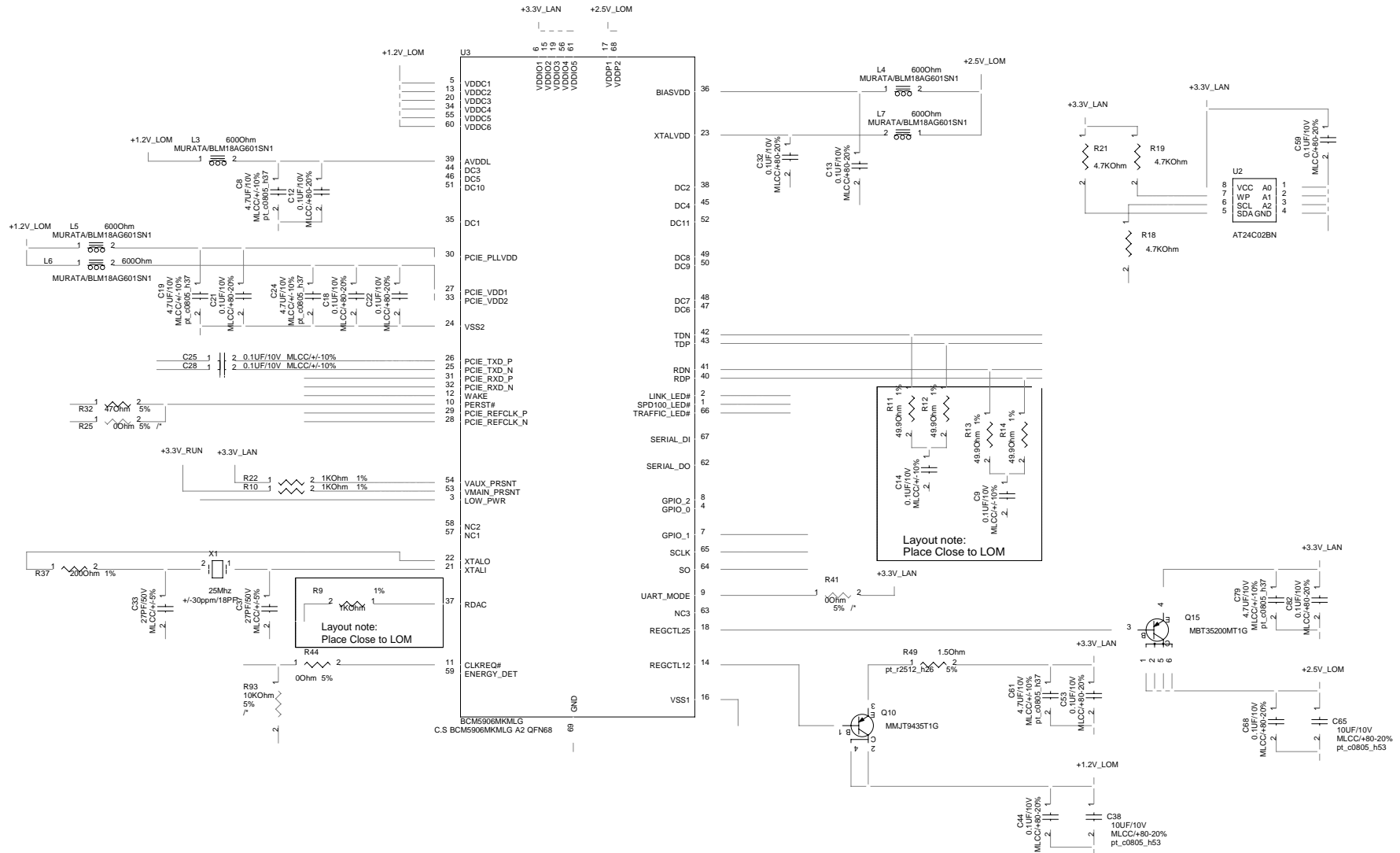
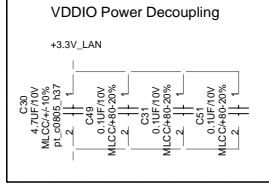
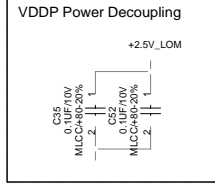
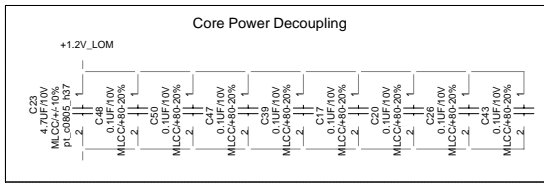
Gain1	Gain2	Gain
0	0	6 dB
0	1	10 dB
1	0	15.6 dB
1	1	21.6 dB

Maxim: 1.8V ~ 3.6V
 TI: 1.8V ~ 4.5V

NOTE: MAKE SURE THERMAL PAD
 (Pin21) UNDER MAX4411 IS NOT
 CONNECTED TO GND



PROJECT: Lanai	REVISION	DATE: Monday, March 19, 2007	DESCRIPTION:	SCHEMATIC FILE NAME :	DESIGN ENGINEER :
	1.2	SHEET OF 68	AMP MAX4411 & AUDIO JACKS	<OrgName>	Yihao Yeh



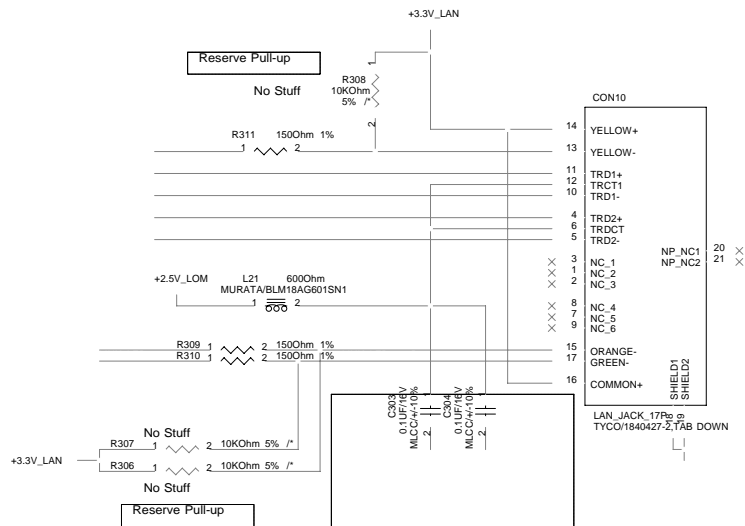
PROJECT: Lanai

REVISION 1.2
DATE: Monday, March 19, 2007
SHEET OF 68

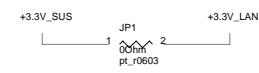
DESCRIPTION:
LAN BCM5906M KMLG(QFN-68)

SCHEMATIC FILE NAME : <OrgName>
RELEASE DATE :

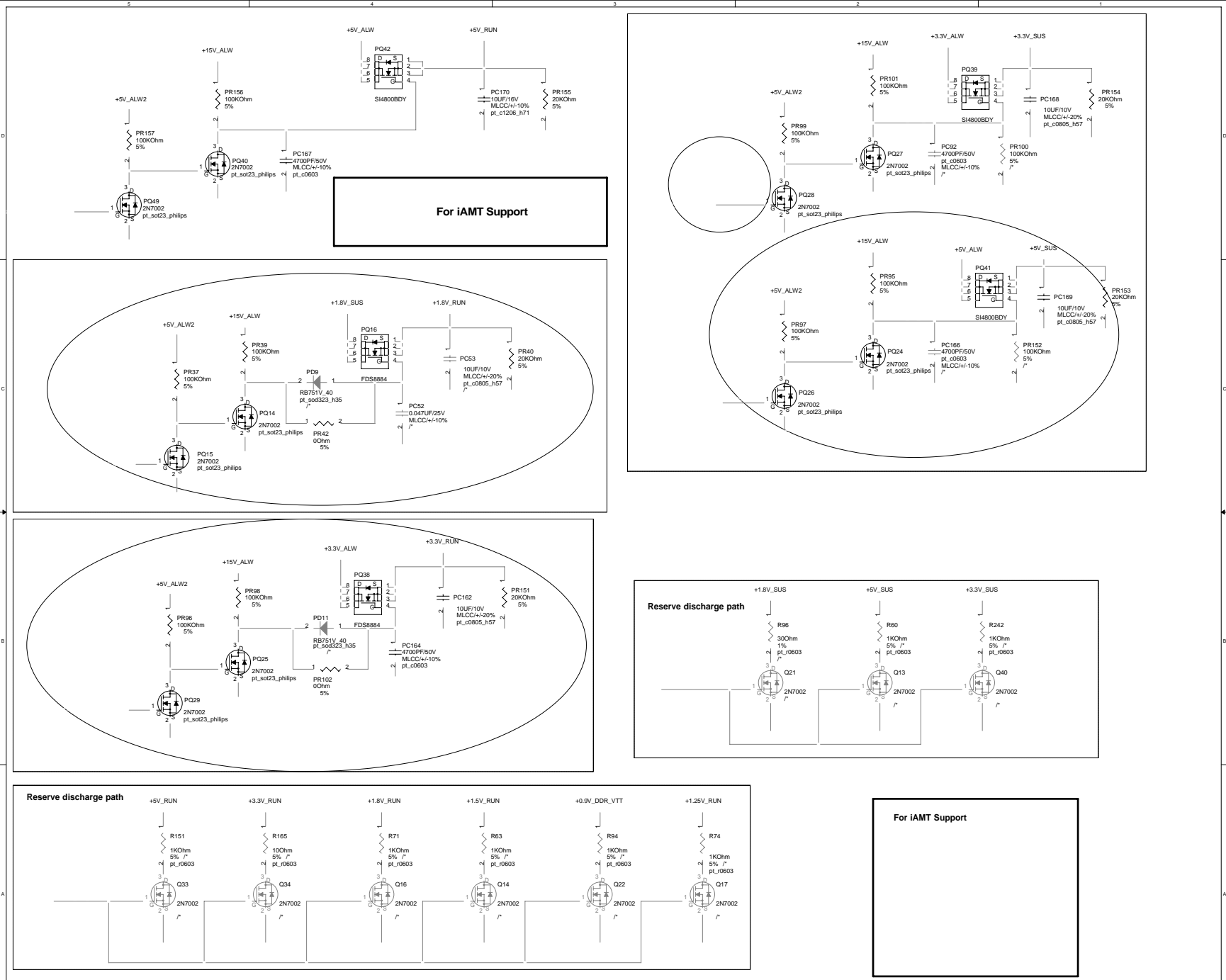
DESIGN ENGINEER :
Ivan Chou

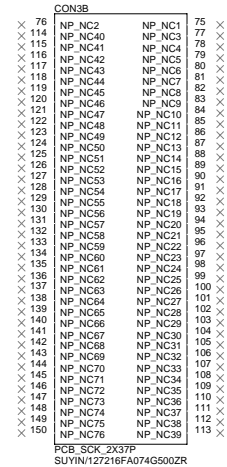
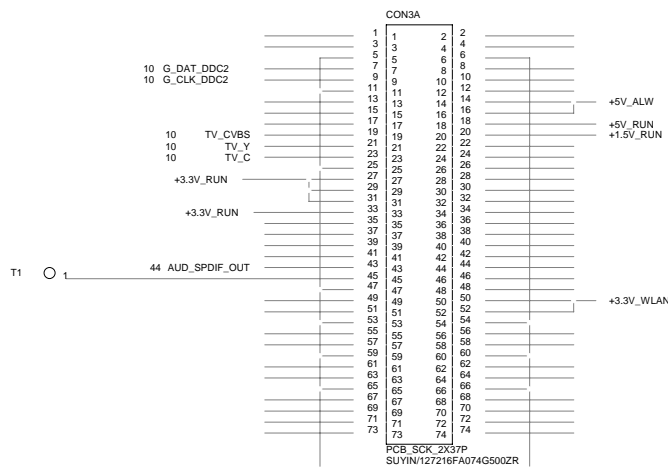
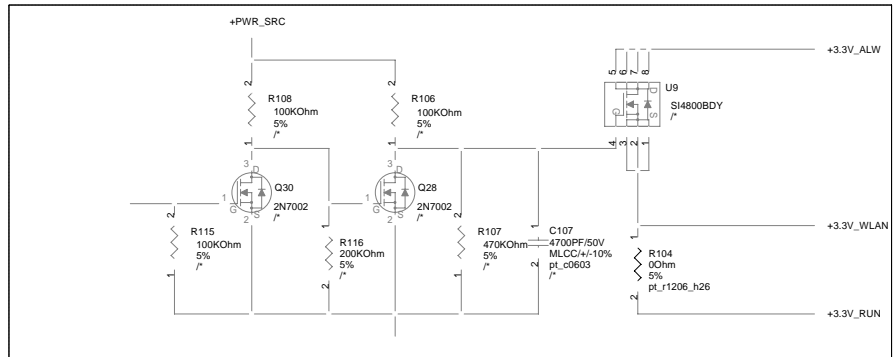


+3.3V_LAN Source Guideline:
 1. Use +3.3V_SUS if Wake-on-LAN is NOT required out of S4, S5
 2. Use +3.3V_SRC if Wake-on-LAN is required out of S4, S5



PROJECT: Lanai	REVISION	DATE: Monday, March 19, 2007	DESCRIPTION:	SCHMATIC FILE NAME :	DESIGN ENGINEER :
	1.2	SHEET OF 68	Magnetics and RJ-45	<OrgName>	Ivan Chou
				RELEASE DATE :	





PCB_SCK_2X37P
SUVIN/127216FA074G5002R

PCB_SCK_2X37P
SUVIN/127216FA074G5002R

PROJECT: Lanai

REVISION
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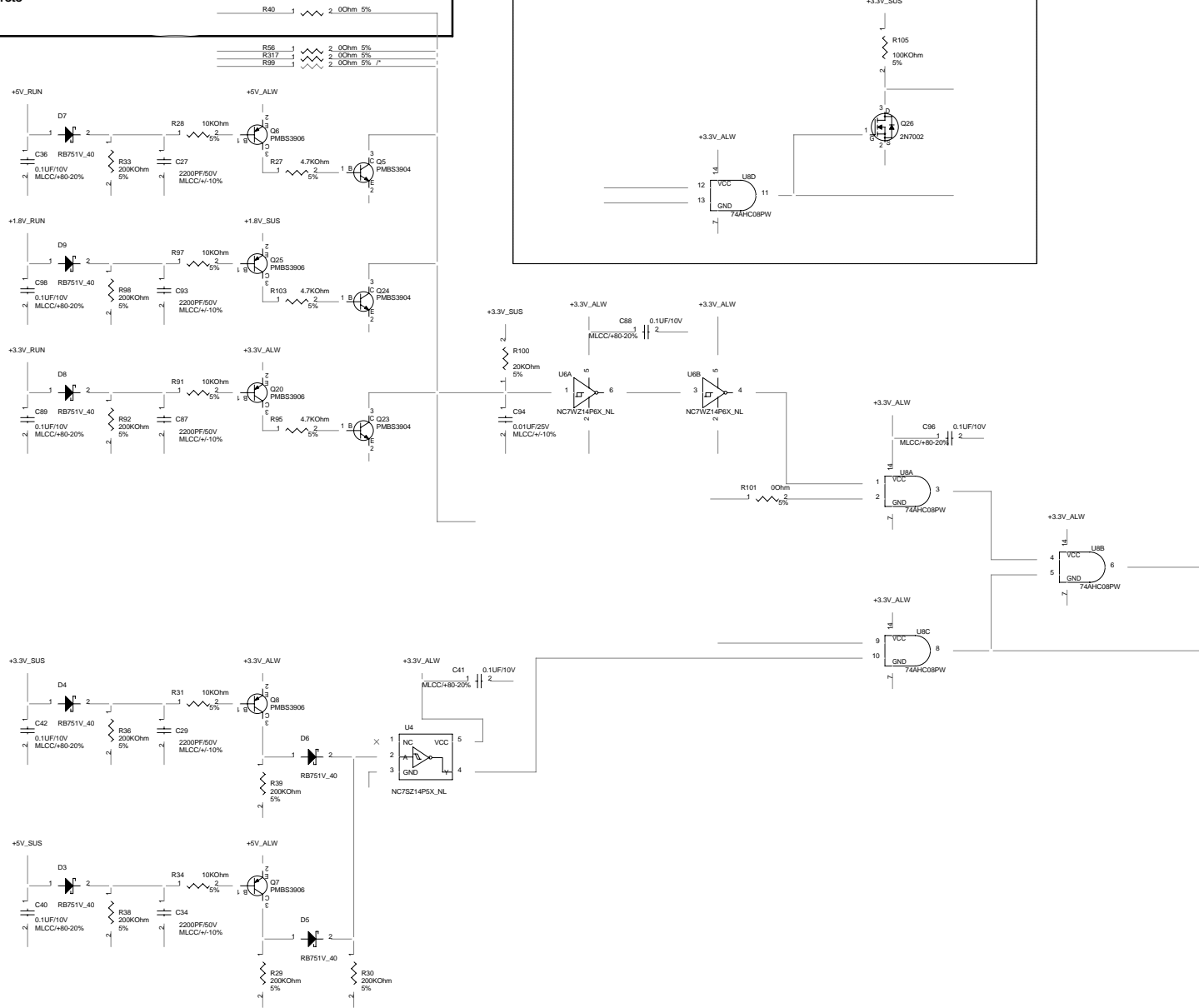
DATE: Monday, March 19, 2007
SHEET OF 68

DESCRIPTION: **BtoB CON**

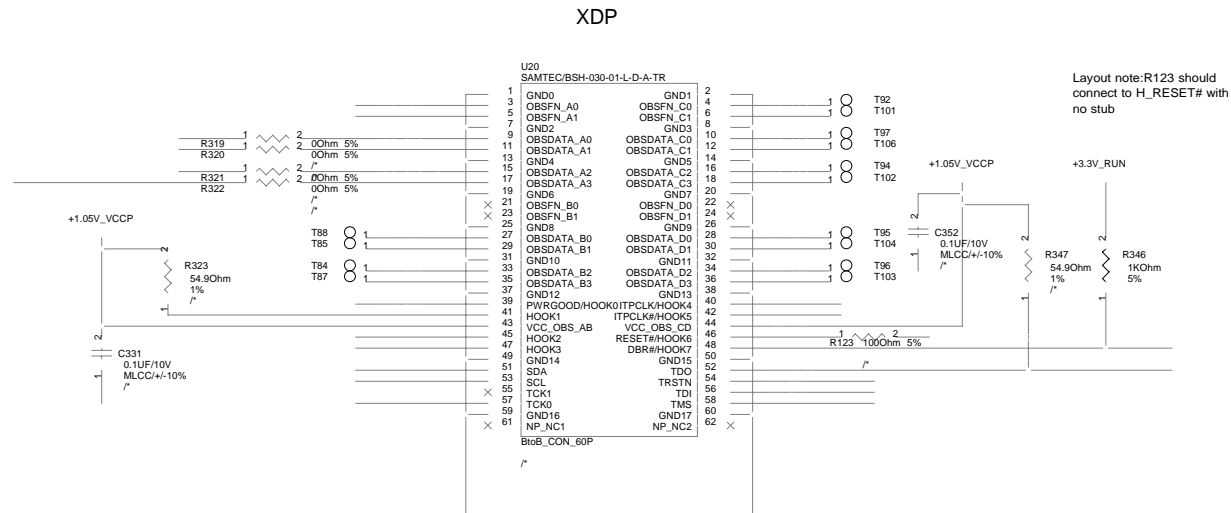
SCHEMATIC FILE NAME : <OrgName>
RELEASE DATE :

DESIGN ENGINEER :
STANLY HSU

Discrete



PROJECT: Lanai	REVISION: 1.2	DATE: Monday, March 19, 2007	DESCRIPTION: Power Sequence Logic	SCHEMATIC FILE NAME:	DESIGN ENGINEER: C.L. Ho
		SHEET OF 68		RELEASE DATE:	

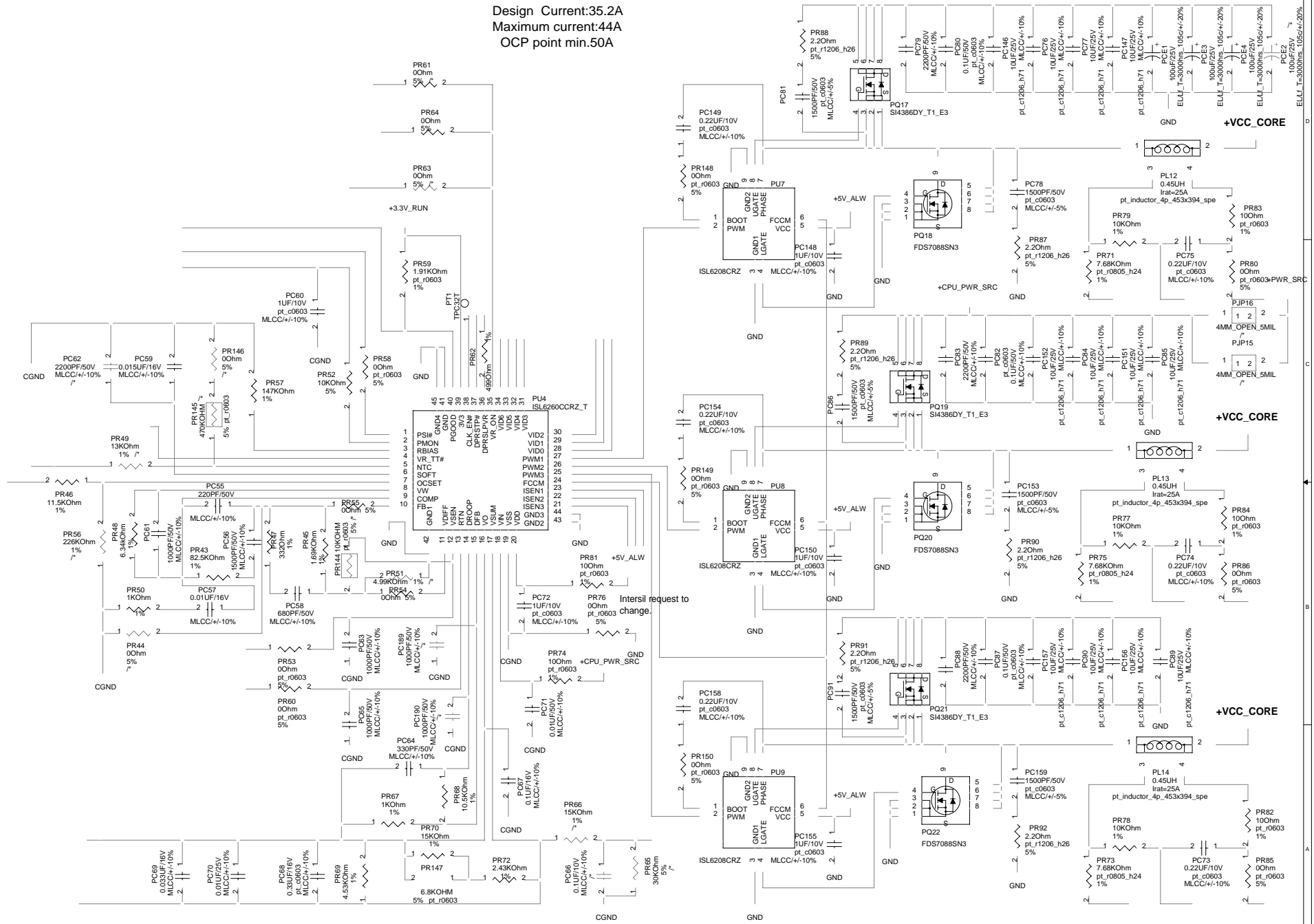


Layout note: R123 should connect to H_RESET# with no stub

CAD NOTE:
Place the XDP connector on the primary side of the CRB and place all components near the connector.

PROJECT: Lanai	REVISION	DATE: Monday, March 19, 2007	DESCRIPTION:	SCHMATIC FILE NAME :	<OrgName>	DESIGN ENGINEER :
	1.2	SHEET OF 68	XDP	RELEASE DATE :		Terry Lin

Design Current:35.2A
 Maximum current:44A
 OCP point min.50A



PROJECT: Lanai

REVISION	DATE: Monday, March 19, 2007
1.2	SHEET OF 68

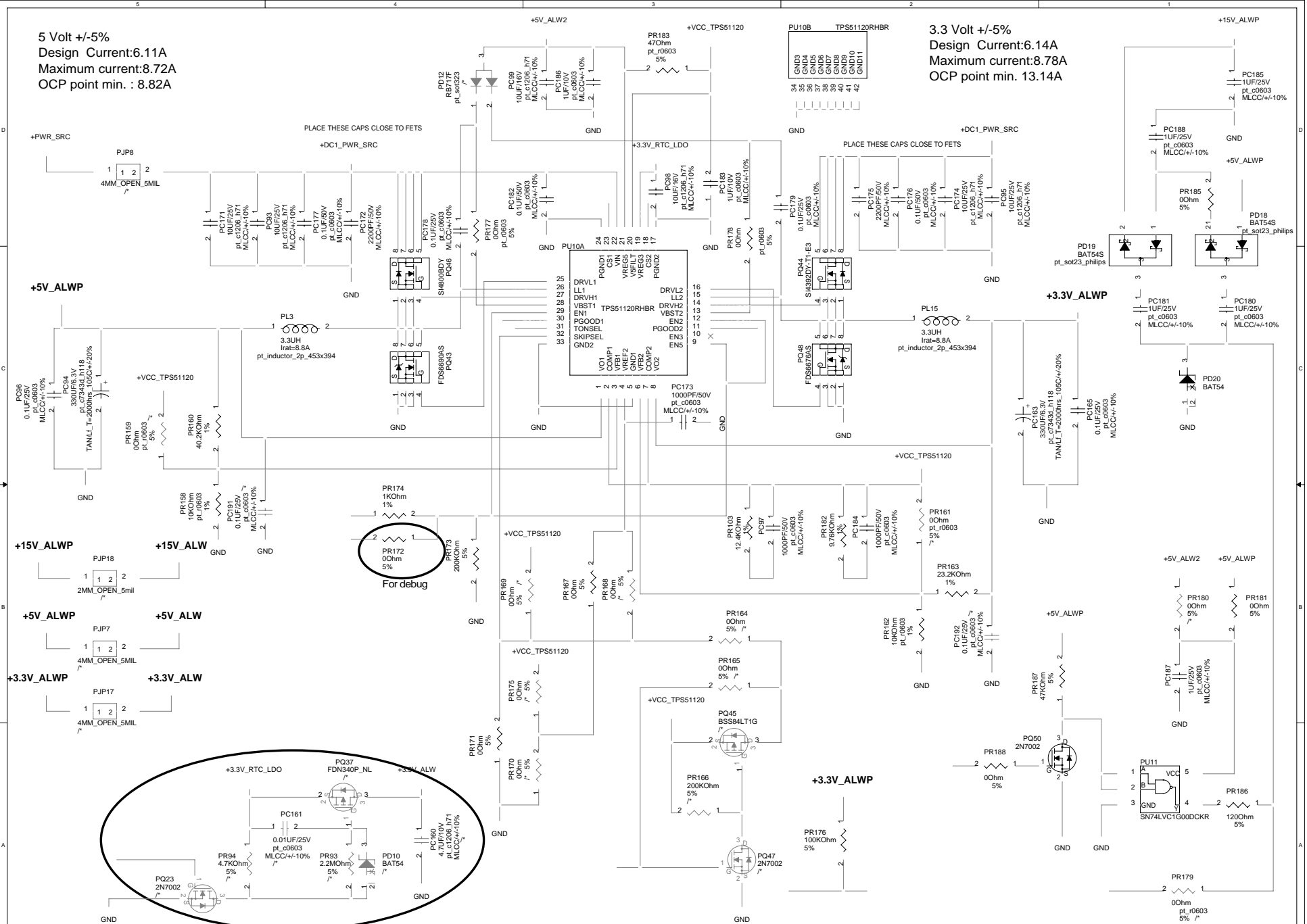
DESCRIPTION: **POWER_VCORE**

SCHEMATIC FILE NAME : <OrgName>
 RELEASE DATE :

DESIGN ENGINEER : **JEFF**

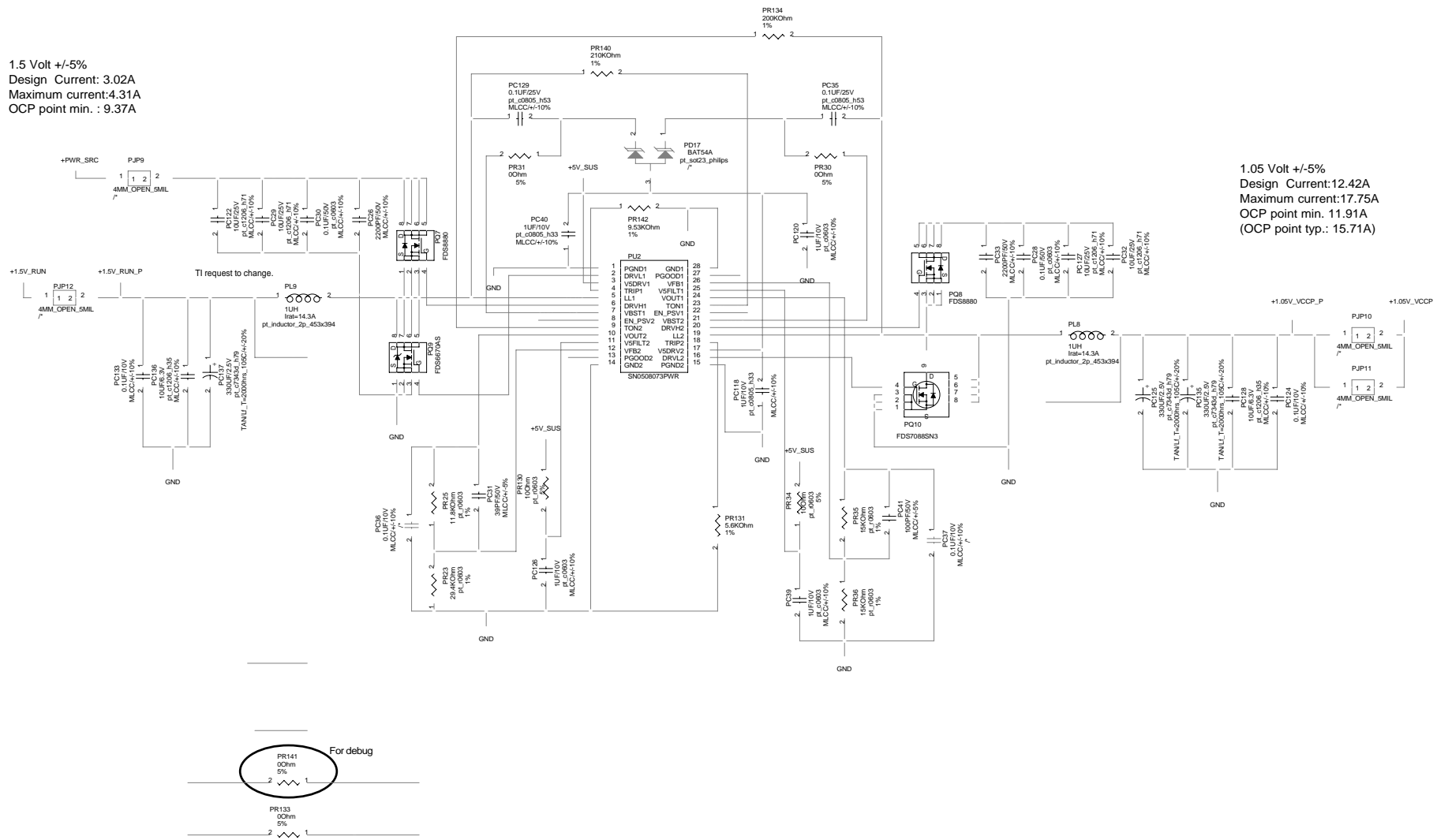
5 Volt +/-5%
 Design Current:6.11A
 Maximum current:8.72A
 OCP point min. : 8.82A

3.3 Volt +/-5%
 Design Current:6.14A
 Maximum current:8.78A
 OCP point min. 13.14A



PROJECT: Lanai	REVISION	DATE: Monday, March 19, 2007	DESCRIPTION:	SCHMATIC FILE NAME :	DESIGN ENGINEER :
	1.2	SHEET OF 68	POWER_SYSTEM 5V_ALW&3.3V_ALW	<OrgName>	JEFF
				RELEASE DATE :	

1.5 Volt +/-5%
 Design Current: 3.02A
 Maximum current: 4.31A
 OCP point min. : 9.37A



1.05 Volt +/-5%
 Design Current: 12.42A
 Maximum current: 17.75A
 OCP point min. 11.91A
 (OCP point typ.: 15.71A)

PROJECT: Lanai	REVISION: 1.2	DATE: Monday, March 19, 2007	DESCRIPTION: POWER I/O 1.5VS & 1.05VS	SCHEMATIC FILE NAME: <OrgName>	DESIGN ENGINEER: JEFF
	SHEET OF 68			RELEASE DATE:	

TOTAL POWER=65W
->3.34A

TABLE3 PIN NAME DIFFERENCES		
PIN	MAXIM	INTERSIL
1	GND	NC
3	REF	VREF
4	CCS	ICOMP
5	CCI	NC
6	CCV	VCOMP
7	DAC	NC
8	IINP	ICM
11	VDD	VDD5MB
14	BATSEL	NC
15	FBSA	VFB
16	FBSB	NC
17	CSIN	CSON
18	CSIP	CSOP
20	DLO	LGATE
21	LDO	VDDP
23	LX	PHASE
24	DHI	UGATE
25	BST	BOOT

"NC" means no-connect

TABLE2 MAXIM & INTERSIL BOM DIFFERENCES		
REF DES	MAXIM	INTERSIL
PR125	8.45K, 0402, 1%	16.0K, 0402, 1%
PC115	0.01uF	No Stuff
PC17	0.1uF, 0402, 10V	No Stuff
PC24	1.0uF, 0603, 10V	No Stuff
PR108	365K, 0402, 1%	215K, 0402, 1%
PR8	0, 0402, 5%	10, 0402, 5%
PR21	0, 0402, 5%	10, 0402, 5%
PC4	No Stuff	0.22uF
PC19	No Stuff	0.22uF
PC22	0.01uF	No Stuff
PC18	0.1uF, 0402, 10V	No Stuff
PC8	220pF, 0402, 50V	No Stuff
PD16	RB751V-40	No Stuff
PC13	3.3nF	No Stuff
PR19	1, 0603, 1%	0, 0603, 5%
PR9	100, 0402, 5%	0, 0402, 5%
PR22	4.7K, 0402, 5%	4.7K, 0402, 5%
PC23	0.01uF	0.01uF
PC21	0.01uF	0.01uF
PD3	1S355	No stuff
PR12	1K, 0603, 5%	No stuff

Charge Current:4.68A
Discharge current:6.6A

TABLE1					
ADAPTOR (W)	TRIP CURRENT (A)	PR121	PR123	PR126	PR122
65	3.17	57.6K	13.0K	105	N/A
90	4.43	51.1K	17.8K	348	33.2K
130	6.43	32.4K	20.5K	100	27.4K
150	7.43	30.9K	24.9K	432	88.7K
200	9.75	19.1K	28K	301	36.5K
230	11.28	32.4K	6.49K	115	N/A

Note 1: PR122 is populated if ADAPT_TRIP is used to program for the next lower adaptor
ADAPT_TRIP_SET is floating for the higher adaptor, grounded for the lower adaptor
Note 2: 24.9K at PR122 allows the 65W adaptor setting to switch down to 45W. (now is N/A)
Note 3: PR109 must be 5m ohm instead of for the 230W adaptor

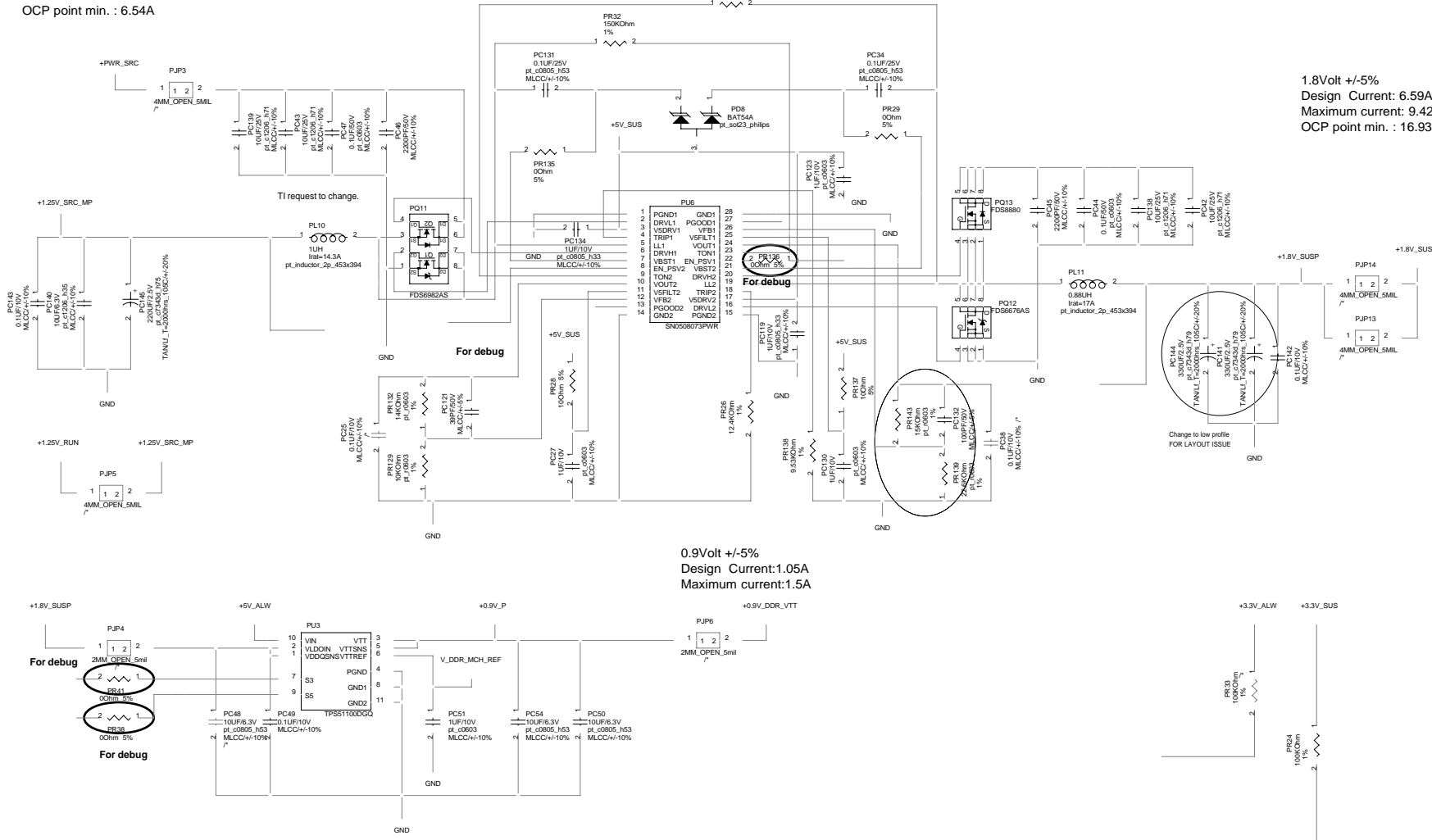
P_SET is
10m ohm

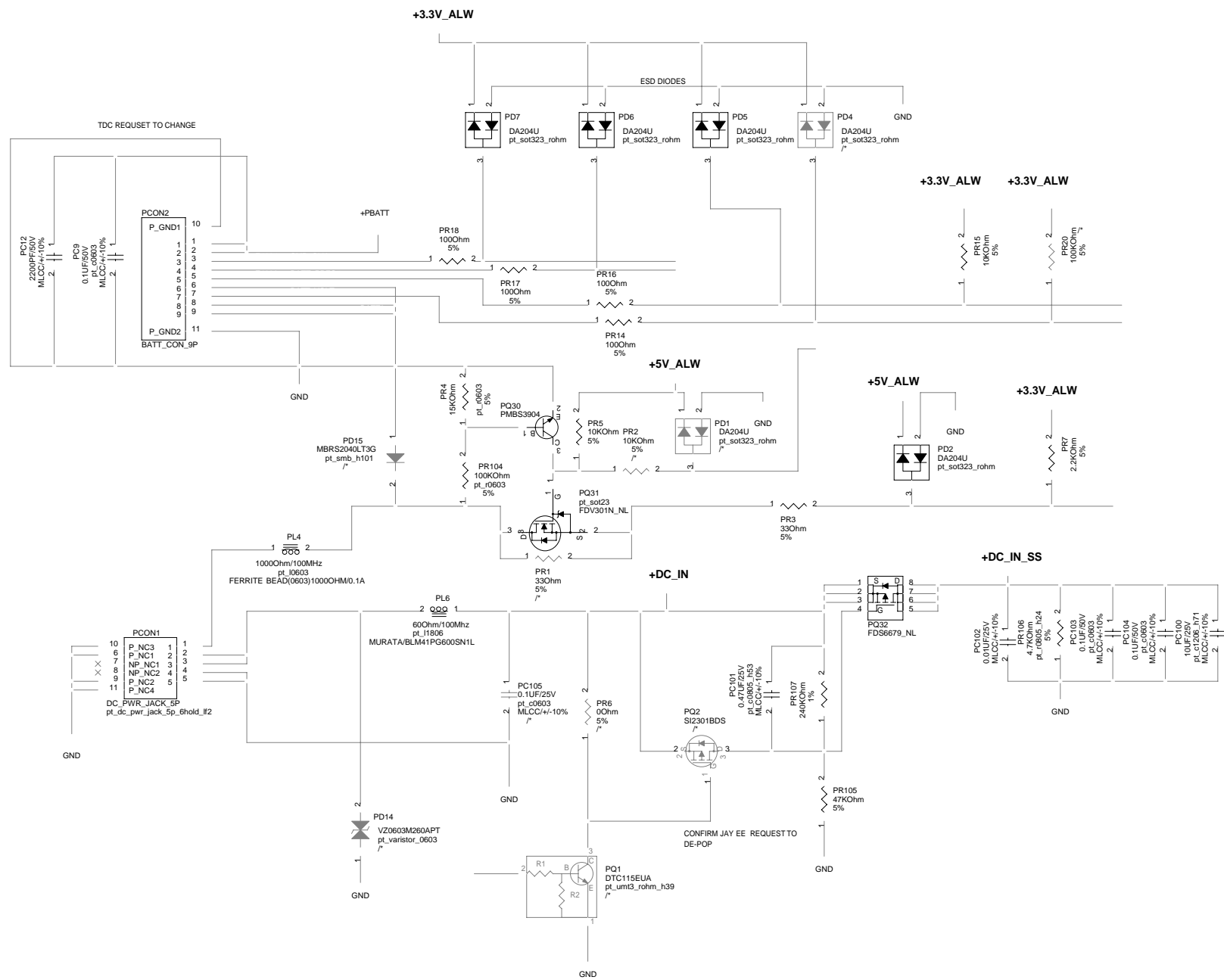
www.laptop-schematics.com

1.25Volt +/-5%
 Design Current:0.93A
 Maximum current:1.33A
 OCP point min. : 6.54A

1.8Volt +/-5%
 Design Current: 6.59A
 Maximum current: 9.42A
 OCP point min. : 16.93A

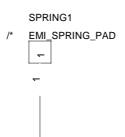
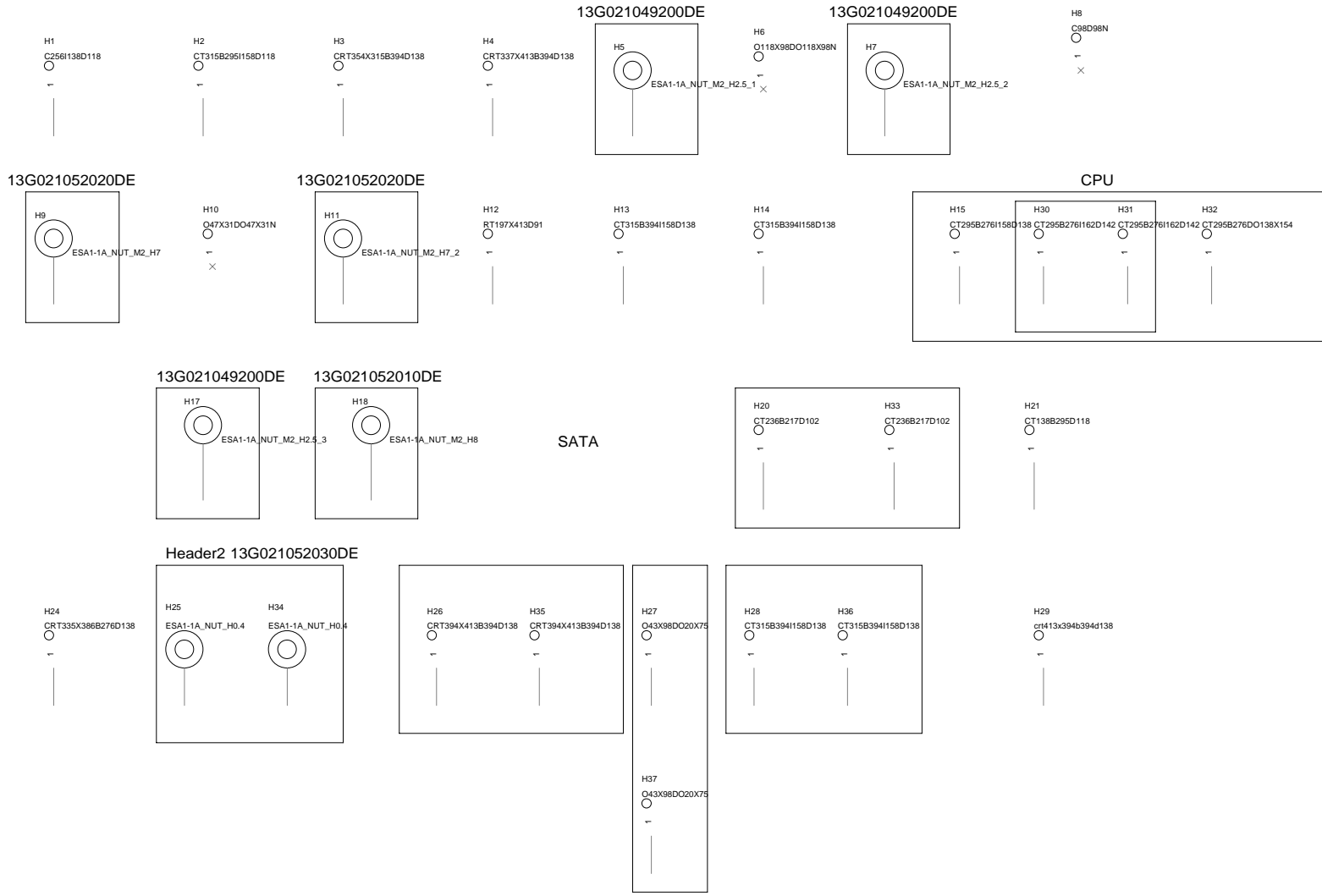
0.9Volt +/-5%
 Design Current:1.05A
 Maximum current:1.5A





PROJECT: Lanai	REVISION	DATE: Monday, March 19, 2007	DESCRIPTION:	SCHMATIC FILE NAME :	DESIGN ENGINEER :
	1.2	SHEET OF 68	POWER_CONNECTOR	<OrgName>	JEFF
				RELEASE DATE :	

GM screw pad

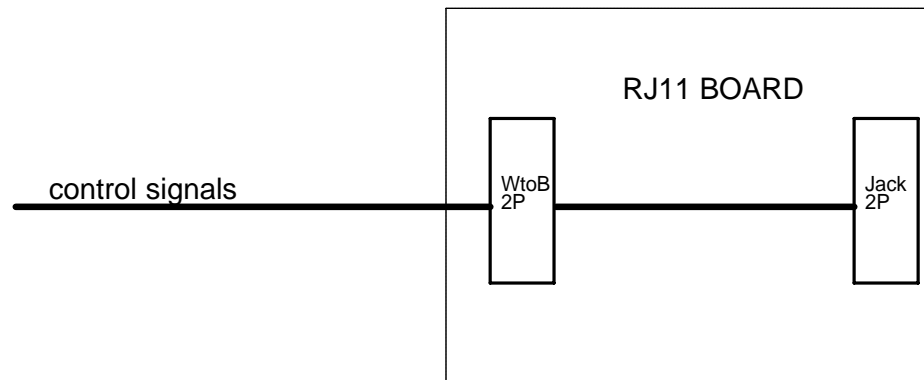


PROJECT: Lanai	REVISION	DATE: Monday, March 19, 2007	DESCRIPTION:	SCHMATIC FILE NAME :	DESIGN ENGINEER :
	1.2	SHEET OF 68	SCREW PAD	RELEASE DATE :	Sean Kuo

ASUS CONFIDENTIAL

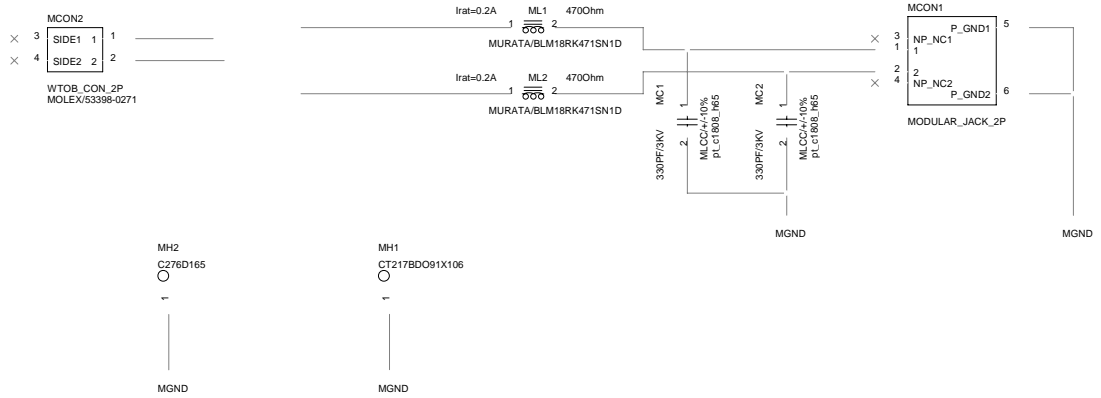
MODEL NAME : Elsa

Lanai:Modem Board



REV : 1.1(DELL: X01)

PROJECT: Lanai	REVISION	DATE: Monday, March 19, 2007	DESCRIPTION:	SCHMATIC FILE NAME :	DESIGN ENGINEER :
	1.2	SHEET OF 68	BLOCK DIAGRAM	RELEASE DATE :	Stanly Hsu



PROJECT: Lanai	REVISION	DATE: Monday, March 19, 2007	DESCRIPTION:	SCHEMATIC FILE NAME :	DESIGN ENGINEER :
	1.2	SHEET OF 68	RJ-11 CONN	<OrgName>	Stanly Hsu
				RELEASE DATE :	

ASUS CONFIDENTIAL

MODEL NAME : Elsa
PCB NO : ???
ASUS P/N : ???

Lanai PP2 USB Board

REV : 1.1(DELL: X01)

MB PCB	
Part Number	Description
DA800004H0L	PCB 00B LA-3071P REV0 MB

BOM NO. ???
PCB P/N: ???

PROJECT: Lanai

REVISION
1.2

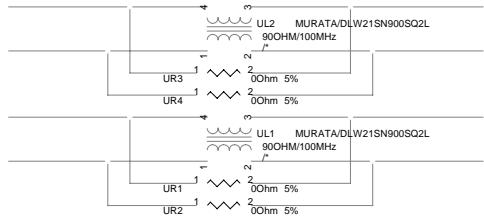
DATE: Monday, March 19, 2007
SHEET OF 68

DESCRIPTION: Cover Page

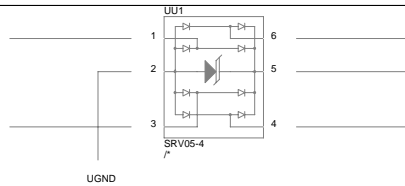
SCHEMATIC FILE NAME :
RELEASE DATE :

DESIGN ENGINEER :
Terry Lin

External USB PORT hookup reference. Your design may need more or less external ports and may be mapped differently .

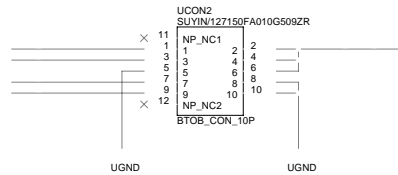


Platforms should put in PADS for the USB chokes if they have the room. Chokes should be NOPOP.

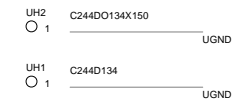


Place ESD diodes as close as USB connector. Semtech SRV05-4 can also be used but the Philips IP42220C26 have a lower input C (1pf vs 3pf).

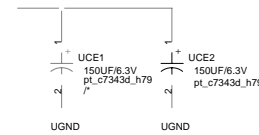
USB daughter board connector



Screw hole

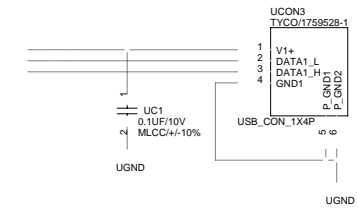
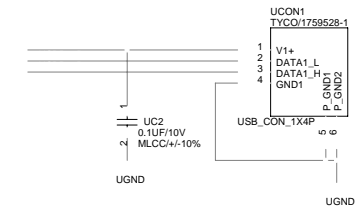


Place one 150uF cap by each USB connector



Each channel is 1A

Consult you ESD Engineer if you think you may need to add ESD Supression Components to your USB lines. Add PADS ONLY until proven diodes are really needed.



PROJECT: Lanai	REVISION	DATE: Monday, March 19, 2007	DESCRIPTION:	SCHEMATIC FILE NAME :	<OrgName>	DESIGN ENGINEER :
	1.2	SHEET OF 68	USB PORT (SINGLE * 2)	RELEASE DATE :		Terry Lin