

Digital command inverts signal

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Many digital designs require voltage-controlled signal inversion. The circuit shown here accepts bipolar inputs with amplitudes up to ± 7 volts and has a gain of either $+1$ or -1 , depending on the logic level at the control terminal. A TTL-logic level of 1 produces a gain of $+1$ (no inversion of the input signal), and a logic level of 0 produces a gain of -1 (signal inversion). The circuit uses a 741 operational amplifier and two transistors.

When the control logic is high, both Q_1 and Q_2 are turned off, and the operational amplifier becomes a voltage follower. The input signal E_i is present at both input terminals and at the output terminal of the op amp, so no current flows through resistors R_1 , R_2 , or R_3 . Therefore the gain in this logic-low mode is independent of the values of the resistors and is given by

$$E_o/E_i = +1$$

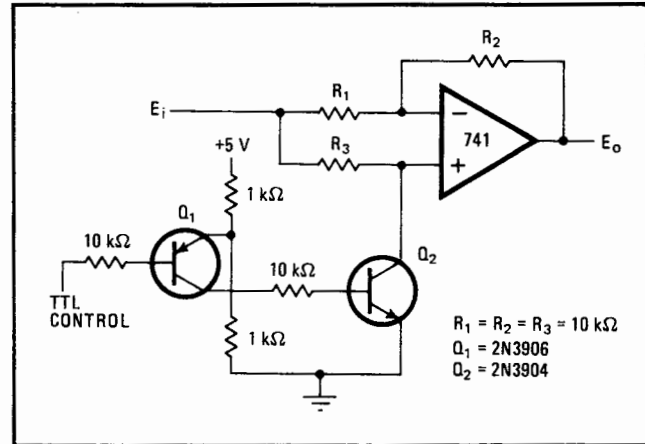
When the control logic is low, both Q_1 and Q_2 are saturated, so the noninverting terminal of the op amp is grounded and the input signal is applied only to the inverting terminal. Therefore the gain is

$$E_o/E_i = -R_2/R_1$$

In this circuit R_1 and R_2 are equal, and therefore the gain in this logic-low mode is

$$E_o/E_i = -1$$

In this mode of operation, there is an offset proportional



Voltage-controlled inverter. Circuit transmits or inverts input signal, depending on logic level at control terminal. Logic 1 produces a gain of $+1$ (no inversion), and logic 0 produces gain of -1 (inversion). Maximum signal swing is ± 7 volts. Offset is about 0.02 volt.

to the saturation voltage of Q_2 :

$$V_{\text{offset}} = V_{\text{sat}}(1 + R_2/R_1) = 0.02 \text{ V}$$

Because this circuit is intended to handle bipolar input signals, Q_2 must be driven by a high-impedance source such as Q_1 , so that Q_2 is turned off by having its base open-circuited, rather than by having its base grounded. If the base of Q_2 were grounded, negative input signals to the circuit would forward-bias the base-to-collector junction and distort the output signal. With the circuit shown here, the negative input swing is limited by the base-to-emitter breakdown voltage of Q_2 (i.e., 6 to 10 V), while the positive input swing is limited only by the op amp saturation voltage. \square